Power Electronic Systems
Laboratory

Electronics Letters, Vol. 60, No. 13, July 2024

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D. Menzi,
A. Yang,
S. Chhawchharia,
J. W. Kolar

ETH zürich

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David Menzi,✉ Aobo Yang, Saransh Chhawchharia, and Johann. W. Kolar
Power Electronic Systems Laboratory, ETH Zurich, Zurich, Switzerland
✉ E-mail: menzi@lem.ee.ethz.ch

Three-phase ac choppers feature output voltage amplitude controllability and enable more compact system realizations compared to autotransformers. For the practical realization advantageously standard power transistor with unipolar voltage blocking capability such as MOSFETs can be employed as a naturally resulting offset voltage between the grid and the input-stage starpoint ensures purely positive power transistor voltages. This offset voltage is, however, not strictly defined and may drift to higher voltage values, resulting in high power transistor voltage stresses and finally a potential overvoltage breakdown. Traditionally, the offset voltage drift is prevented by introducing discharge resistors across the input-stage capacitors which, however, results in substantial ohmic losses. This paper analyzes the offset voltage formation in ac choppers and proposes a novel clamping modulation scheme which ensures a strictly defined and minimum time-varying offset voltage without need for discharge resistors. Theoretical analyses and circuit simulations are finally experimentally verified with a 400 V (rms, line-to-line) 50 Hz grid connected three-phase buck-boost ac chopper with 3 kW rated power.

Introduction: Autotransformers enable ac voltage amplitude adjustment in applications where no isolation or grid frequency adjustment is required. Operating at the grid frequency f_g, the required magnetic core volume and weight is large and thus pulse-width modulated (PWM) ac choppers operating at a switching frequency $f_s \gg f_g$ enable substantial weight and volume gains [1, 2].

Single-phase ac choppers were first proposed in the eighties [3–5] and required power switches with bipolar voltage blocking capability (typically realized as an inverse-series connection of two MOSFETs with anti-parallel body diodes and thus unipolar voltage blocking capability). In the following decade the concept of the ac chopper was extended to three-phase systems [6–9] and topologies with buck, boost or buck-boost capability [10–13] were proposed. Advantageously the presence of an offset voltage between the grid starpoint m and the input-stage starpoint n (see Figure 1; the same also applies to the output stage) enables a strictly positive voltage across the power switches and therefore standard MOSFETs with unipolar blocking voltage capability can be employed. The offset voltage u_{mn} is built up automatically upon connection to the grid but is, however, not strictly defined and may drift to higher voltage values during operation, resulting in elevated power transistor voltage stresses and potentially in an overvoltage breakdown. This offset voltage drift is already described in [6] and is addressed there by introducing discharge resistors across the input and output-stage filter capacitors. However, this approach results in substantial ohmic losses of approximately 1% of the processed power, which is obviously undesirable when aiming for high-efficiency power conversion.

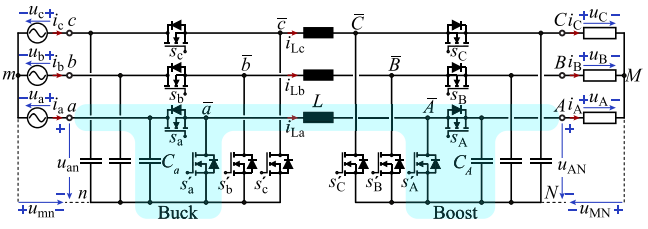

Fig. 1 *Main power circuit of the considered three-phase buck-boost ac chopper from [13] with converter phase a highlighted in light blue: In contrast to the bipolar sinusoidal grid input u_a, u_b, u_c (with frequency f_g and line-to-neutral amplitude $\hat{U}_g$) and output voltages u_A, u_B, u_C (with frequency $f_G = f_g$ and adjustable amplitude $\hat{U}_G$), the input (buck) u_{an}, u_{bn}, u_{cn} and output (boost) stage voltages u_{AN}, u_{BN}, u_{CN} comprise an offset voltage u_{mn} and u_{MN}, respectively, assuring strictly positive (unipolar) voltages across the power semiconductors. Operation with constant PWM duty cycles in the buck or the boost stage results in naturally sinusoidal input i_a, i_b, i_c and output currents i_A, i_B, i_C*

Thus, after reviewing the underlying principle of the offset voltage formation in three-phase ac choppers this paper proposes a novel clamping modulation scheme that results in a strictly defined and minimal time-varying offset voltage without need for discharge resistors. Theoretical analyses and circuit simulations are experimentally verified with a 400 V (rms, line-to-line) 50Hz grid connected three-phase buck-boost ac chopper of 3 kW rated power.

Offset voltage formation and modulation: For completeness, the operating concept of the three-phase buck-boost ac chopper in Figure 1 is briefly recapitulated here and the Appendix provides a more detailed analysis of the basic voltage an current formation. For a given grid line-to-neutral input voltage amplitude $\hat{U}_g$ and a desired output voltage amplitude $\hat{U}_G$ the system operates with a modulation index M which is then translated into PWM duty cycles for the buck input D_{Bu} or the boost output stage D_{Bo} as

$$M = \frac{\hat{U}_G}{\hat{U}_g}, D_{Bu} = \min(M, 1), D_{Bo} = \min(M^{-1}, 1). \quad (1)$$

Advantageously, this modulation results in a mutually exclusive operation of the buck and the boost stage [14] where, for example, for $\hat{U}_G < \hat{U}_g$ (buck mode) the boost-stage high-side switches s_A, s_B, s_C are permanently turned on with $D_{Bo} = 1$ (and thus do not create any switching losses). Meanwhile the buck-stage switches operate synchronously with PWM and a relative on-time D_{Bu} of the high-side switches s_a, s_b, s_c (the low-side switching signals for s'_a, s'_b, s'_c are set complimentary) to steps down the input voltage similar to a dc-dc converter [2].

As mentioned, three-phase ac choppers feature inherently positive input (and output) stage voltages and Figure 2 depicts the relevant waveforms of the ac chopper in Figure 1 during startup obtained from a circuit simulation in PLECS [15]:

At the time instance $t = t_1$ the converter is connected to the three-phase grid with a line-to-neutral voltage amplitude $\hat{U}_g = 325$ V (see Figure 2a) via precharge resistors R_p. There, all power transistors are turned off and Figure 3a depicts the relevant current paths during this precharge state: The grid voltages u_a, u_b, u_c impress sinusoidal differential mode (DM) voltages at the input terminals a, b, c (and thus across the capacitors C_a, C_b, C_c) and at the same time the body diodes of the power transistors prevent negative input-stage voltages u_{an}, u_{bn}, u_{cn}. Here the body diodes of the instantaneously most negative phase a start to conduct at $t = t_1$ and thus a common-mode (CM) offset voltage $u_{mn} = \frac{1}{3}(u_{an} + u_{bn} + u_{cn})$ is naturally built up and results to $u_{mn} \approx \hat{U}_g$ (see Figure 2c). Note that u_{mn} is slightly varying over time due to discharge resistors R_d parallel connected to each input (and output) capacitor.

Once the auxiliary circuits (controller, measurements, gate drivers) have started, the relays s_p bypass the precharge resistors and the converter begins PWM operation at $t = t_2$ and ramps up the output voltages u_A, u_B, u_C and currents i_A, i_B, i_C. Steady-state operation with $\hat{U}_G = \hat{U}_g/2$ (or any other desired value) is reached at $t = t_3$.

Figure 2c.i depicts the resulting input-stage voltages u_{an}, u_{bn}, u_{cn} for conventional modulation where the offset voltage u_{mn} begins to drift towards 400 V with the beginning of the PWM operation at $t = t_2$. This results in elevated power transistor blocking voltage $\hat{u}_{SPWM}$ of approximately 725 V but does not negatively impact the generated output voltages, as u_{mn} represents a CM voltage component which cannot drive any currents into the open-starpoint load. As discussed in [6] the culprit for this offset deviation is the PWM interlock delay / dead time of duration t_d (occurring twice every switching period $T_s = 1/f_s$) during which both high-side and low-side power transistors of the input stage are in off state. The resulting current paths during the interlock delay time for $t = t_3$ where $i_{La} < 0$ A and $i_{Lb}, i_{Lc} > 0$ A are depicted in Figure 3b and similarly to the precharge interval the diode conduction leads to an inherent increase of the offset voltage u_{mn} which scales with both, the output current amplitude $\hat{I}_G$ and the relative duration of the dead-time t_d/T_s [6]. Ref. [6] provides design guidelines for the selection of suitable discharge

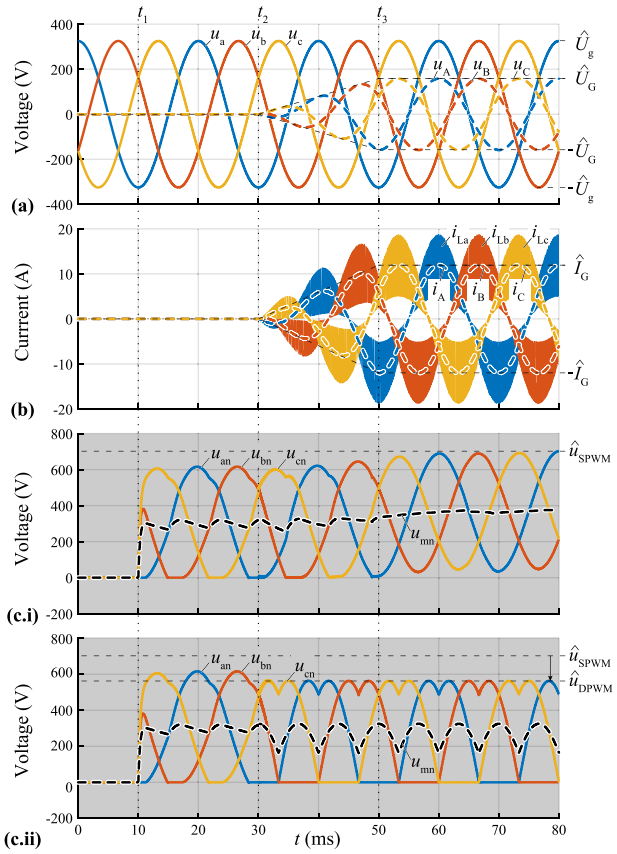

Fig. 2 *Simulated converter waveforms during system startup: (a) grid input u_a, u_b, u_c (with frequency $f_g = 50$ Hz and line-to-neutral amplitude $\hat{U}_g = 325$ V, i.e. 230 V_{rms}) and output voltages u_A, u_B, u_C (with frequency $f_G = f_g$ and a steady-state amplitude $\hat{U}_G = \hat{U}_g/2$, that is, a modulation index $M = \hat{U}_G/\hat{U}_g = 0.5$), (b) sinusoidal output currents i_A, i_B, i_C (with a steady-state amplitude $\hat{I}_G = 12.3$ A) and buck-boost inductor currents i_{La}, i_{Lb}, i_{Lc}, and (c) input-stage voltages u_{an}, u_{bn}, u_{cn} comprising an offset voltage u_{mn} for (c.i) conventional (continuous) modulation and (c.ii) the proposed clamping modulation. The considered circuit parameters include a switching frequency $f_s = 72$ kHz (with a PWM interlock-delay $t_d = 100$ ns and a power transistor parasitic capacitance $C_{oss} = 0.5$ nF), buck-boost inductors $L = 85$ µH, filter capacitors $C_a = C_A = 2$ µF (with parallel-connected discharge resistors $R_d = 15$ kΩ), and precharge resistors $R_p = 50$ Ω (see Figure 3)*

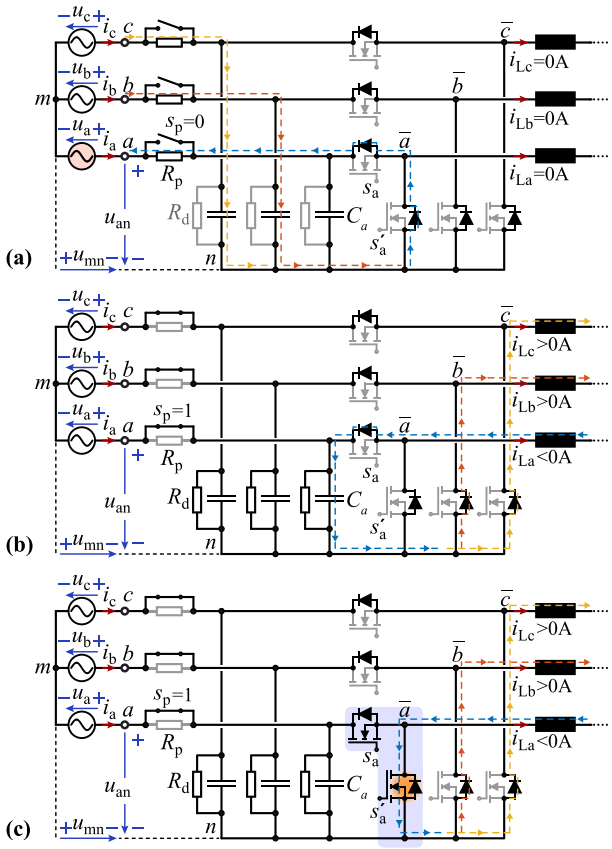

Fig. 3 *Relevant current paths of the converter input stage from Figure 1 during (a) the system precharge state ($t_1 \le t \le t_2$ in Figure 2) and during (b) the PWM interlock-delay time t_d in normal operation ($t > t_2$ in Figure 2) for buck-boost inductor currents $i_{La} < 0$ A and i_{Lb}, $i_{Lc} > 0$ A. Note that before and after the dead-time interval, the symmetric buck-boost inductor currents i_{La}, i_{Lb}, i_{Lc} sum to zero via either the high-side power transistors s_a, s_b, s_c or the low-side power transistors s'_a, s'_b, s'_c due to the synchronous PWM operation and no offset-voltage build-up takes place. In contrast, during the dead-time interval all high- and low-side power transistors are turned off. Thus the current paths are defined by the sign of the buck-boost inductor currents and an offset-voltage build-up in the phases with instantaneously negative buck-boost inductor currents takes place. The current paths during the dead time interval for DPWM operation are further highlighted in (c) where the switches of the instantaneously most negative phase (here s_a and s'_a of phase a), are permanently turned on, thus preventing an offset voltage build-up*

resistors R_d connected in parallel to the input (and output) stage filter capacitors as indicated in Figure 3b which maintain $u_{mn} \approx \hat{U}_g$. This simple discharge-resistor-based offset voltage control is employed, for example, in [16–19] but results in substantial ohmic losses of approximately 1% of the nominal converter power [6] which is obviously undesirable, especially with respect to the part-load efficiency.

Aiming for high-efficiency power conversion this paper proposes a novel clamping modulation strategy as highlighted in Figure 2c.ii where the phase with the instantaneously most negative grid voltage simultaneously turns on both, the high-side and the low-side switch for one third of the grid period $T_g = 1/f_g$, thereby connecting the input-stage reference potential n to the corresponding grid terminal (the Appendix provides a detailed comparison to the conventional (continuous) modulation). This clamping modulation thus represents a discontinuous PWM (DPWM) operation strategy and the time-varying u_{mn} is now strictly defined as

$$u_{mn}(t) = -\min(u_a(t), u_b(t), u_c(t)). \tag{2}$$

Thus, the maximum power transistor blocking voltage during PWM operation, $\hat{u}_{DPWM} = \sqrt{3}\hat{U}_g = 565$ V, can be limited to the grid line-to-line voltage which enables the safe operation with 900 V power transistor technology. Further, the buck-boost inductor currents i_{La}, i_{Lb}, i_{Lc} cancel out in the input stage starpoint n during the dead-time interval illustrated in Figure 3c without causing an offset voltage increase, thus rectifying the root cause of the undesired (and uncontrolled) offset voltage build-up. In consequence, the $R_p = 15$ kΩ discharge resistors considered in Figure 2 to maintain a minimum constant offset $u_{mn} \approx \hat{U}_g$ for the conventional modulation can be omitted, thereby reducing the losses by 43.2 W corresponding to 1.4% of the 3 kW nominal converter power. It is worth highlighting that the clamping modulation also results in a switching loss reduction due to the 1/3 lower number of switching actions, which is, however, rather minute as the clamping interval in each phase occurs when the switched voltage (e.g. u_{an} in phase a) is already low in the conventional (continuous) modulation. To avoid a sudden jump in the offset voltage u_{mn} and the input-stage capacitor voltages the beginning of the modulation is timed to $t = t_2$ where $u_a = -\hat{U}_g$ and such that the input capacitor voltage is already $u_{an} = 0$ V when s_a and s'_a are both turned on. In doing so, transients oscillations during system startup can be avoided.

Experimental verification: To verify the proposed clamping modulation a 3 kW hardware demonstrator according to the specifications in Figure 2 is constructed. SiC MOSFETs (C3M0010090K) with 900 V voltage rating are employed which provide sufficient blocking voltage margin for $\hat{u}_{DPWM} = 565$ V resulting in the European 400 V (rms, line-to-line) three-phase grid.

Figure 4a provides experimental waveforms with conventional modulation where at $t = t_2$ the PWM operation is started (compare $t = t_2$ in Figure 2) and the output voltage is ramped up during 100 ms.

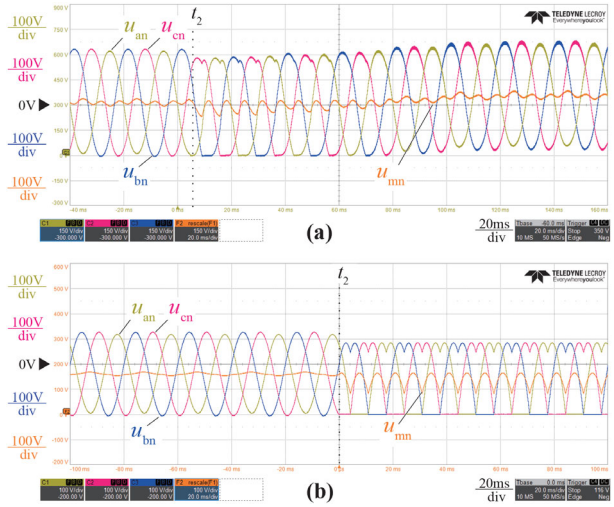

Fig. 4 *Experimental waveforms during system startup for (a) the standard (continuous) and (b) the proposed clamping modulation for a line-to-neutral grid voltage amplitude* $\hat{U}_g = 325\,\mathrm{V}$*, that is,* $230\,\mathrm{V_{rms}}$*: The input-stage voltages* u_{an}, u_{bn}, u_{cn} *are measured with differential probes and their offset voltage* u_{mn} *is obtained with a math channel. The main hardware demonstrator circuit parameters are identical to Figure 2*

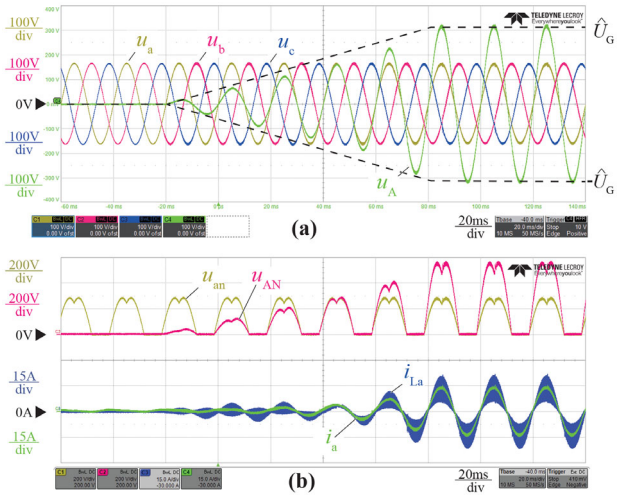

Fig. 5 *Transient buck-boost operation for a constant input voltage amplitude* $\hat{U}_g = 165\,\mathrm{V}$ *(*$\approx 115\,\mathrm{V_{rms}}$*) and an output voltage amplitude* $\hat{U}_G$ *which is ramped up from* 0 V *to* 325 V*: In (a) the sinusoidal grid input voltages* u_a, u_b, u_c *and the generated phase a output voltage* u_A *can be observed. A second oscilloscope (b) is triggered synchronously and depicts the detailed waveforms of the converter phase a, namely the input-* u_{an} *and output-stage voltage* u_{AN} *with the characteristic zero-volt clamping intervals, as well as the grid input current* i_a *and the buck-boost inductor current* i_{La}

As predicted by the simulations, the offset voltage u_{mn} is not strictly defined and reaches elevated values towards 400 V in steady-state operation. In contrast the proposed clamping modulation presented in Figure 4b results in the predicted time-varying minimum offset voltage u_{mn} and substantially reduced power transistor blocking voltage stresses. Note that no transient oscillations result in the beginning of each clamping interval.

Figure 5 further presents experimental waveforms with focus on converter phase *a* in buck-boost operation where for a grid input voltage $\hat{U}_g = 165\,\mathrm{V}$ ($\approx 115\,\mathrm{V_{rms}}$) the output voltage $\hat{U}_G$ is ramped up from 0 V to 325 V. There, the proposed clamping logic is applied to both, the input and the output stage and the characteristic voltage shape of u_{an} and u_{AN} with zero-voltage intervals during 1/3 of the grid period can be observed. As can be noted, the grid input current i_a is fully sinusoidal and a smooth transition from buck to boost operation can be achieved, thus verifying the proposed clamping modulation scheme.

Conclusion: Three-phase ac choppers enable ac voltage amplitude adjustment (without frequency adjustment and isolation) and allow for a compact system realization compared to autotransformers. Advantageously, three-phase ac choppers can employ standard MOSFETs with unipolar blocking voltage capability due to an offset voltage which is naturally established between the grid and the input-stage starpoint. The offset voltage is, however, not strictly defined and dangerously high voltage levels may results in operation. The novel clamping modulation proposed and verified in this paper assures operation with a strictly defined and minimum offset voltage, which is a major improvement over the state-of-the art offset voltage control based on discharge resistors which are causing relatively large power losses and resulting in limited conversion efficiency, especially in part-load operation.

Author contributions: **David Menzi**: Conceptualization; data curation; formal analysis; investigation; methodology; project administration; software; supervision; visualization; writing—original draft; writing—review and editing. **Aobo Yang**: Formal analysis; investigation; software; validation; visualization; writing—original draft. **Saransh Chhawchharia**: Conceptualization; investigation; methodology; project administration; resources; software; supervision. **Johann W. Kolar**: Conceptualization; funding acquisition; methodology; project administration; resources; supervision; writing—review and editing.

Conflict of interest statement: The authors declare no conflicts of interest.

Data availability statement: Data available on request from the authors

Received: *22 January 2024* Accepted: *20 April 2024*
doi: 10.1049/ell2.13210

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Appendix:

AC chopper voltage and current formation: The goal of this Appendix is to provide details on the basic voltage and current formation of the ac chopper in Figure 1 and to compare the PWM switching patterns of the conventional (continuous) and the DPWM / clamping modulation.

In Figure A1, the waveforms (generated in MATLAB) for conventional modulation and buck operation are displayed. A low switching frequency $f_s = 24 f_g$ is selected for illustration purposes, whereas for the practical realization $f_s \gg f_g$ is selected to minimize the size of the passive components. Here, the input-stage half-bridges are switched synchronously with a constant duty cycle D_{Bu} for the high-side power transistors defined by (1) (Figure A1b). The generated switch-node voltages $u_{\bar{a}n}, u_{\bar{b}n}, u_{\bar{c}n}$ (Figure A1c) comprise a CM component which cannot drive any current in the open-starpoint system. Further, the resulting high-frequency DM voltage-time area in phase *a* (causing a high-frequency current ripple in the buck-boost inductor) is highlighted and the low-frequency DM voltage component is (in first approximation) equal to the output voltage u_A. Figure A1d further illustrates the buck-boost inductor currents i_{La}, i_{Lb}, i_{Lc}. In buck operation the output stage high-side switches s_A, s_B, s_C are constantly on, such that the low-frequency component of the inductor currents i_{La}, i_{Lb}, i_{Lc} is identical to the output currents i_A, i_B, i_C. For phase *a*, further the power transistor current i_{sa}, $i_{s'a}$ and the resulting low-frequency grid input current i_a are highlighted.

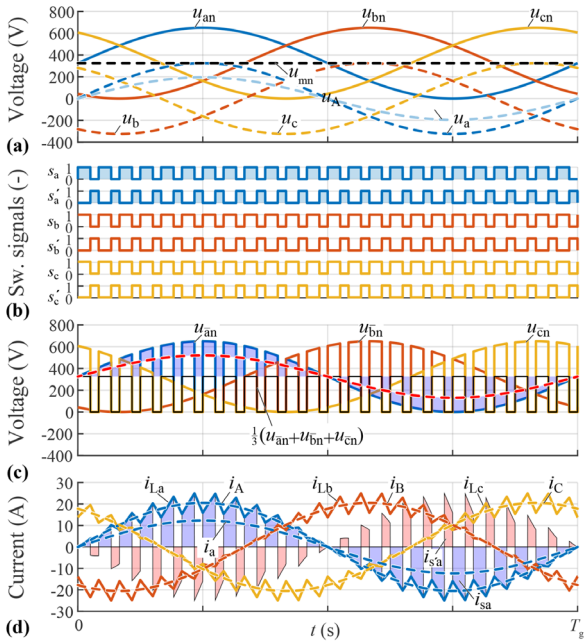

Fig. A1 *Main waveforms of the buck-boost ac-chopper input stage generated in MATLAB during one grid period $T_g = 1/f_g$ for conventional (continuous) modulation with a low switching frequency $f_s = 24 f_g$ in buck operation and a modulation index $M = 0.6$: (a) sinusoidal grid voltages u_a, u_b, u_c (with a line-to-neutral amplitude $\hat{U}_g = 325$ V) and strictly positive (unipolar) converter input voltages u_{an}, u_{bn}, u_{cn} comprising a CM offset voltage $u_{mn} = \hat{U}_g$, (b) switching signals of the input-stage semiconductors, (c) switch-node voltages $u_{\bar{a}n}, u_{\bar{b}n}, u_{\bar{c}n}$ and the resulting CM voltage component $\frac{1}{3}(u_{\bar{a}n} + u_{\bar{b}n} + u_{\bar{c}n})$ (the resulting high-frequency DM voltage-time area in phase a is highlighted), and (d) buck-boost inductor currents i_{La}, i_{Lb}, i_{Lc} and low-frequency output currents i_A, i_B, i_C (for phase a the power transistor currents $i_{sa}, i_{s'a}$ and the resulting low-frequency grid current i_a are highlighted)*

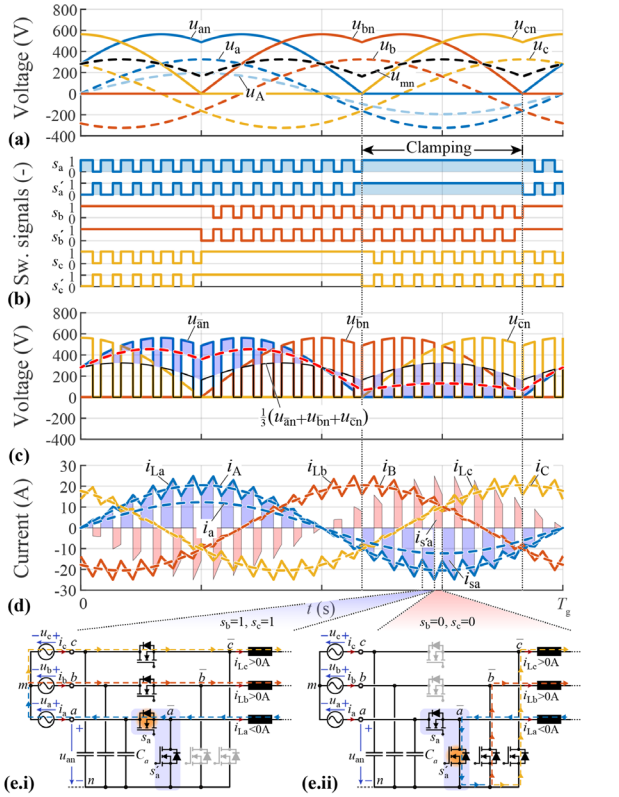

Fig. A2 *Main waveforms for the DPWM / clamping modulation. For comparison to the conventional (continuous) modulation the operating point and the displayed signals in (a)–(d) are identical to Figure A1; (e) further illustrates the current paths in the phase a input stage during the clamping interval*

When applying the DPWM/clamping modulation, a time-varying offset voltage u_{mn} according to (2) is impressed by simultaneously turning on the high-side and low-side power transistor of the phase with the currently most negative grid input voltage as illustrated in Figure A2a,b. Note that in contrast to the standard (continuous) modulation, the DPWM operation results in a low-frequency excitation of the input stage starpoint *n* with respect to ground, which limits the maximally allowed capacitance from *n* to protective earth in the electromagnetic interference filter to approximately 50 nF to comply with the 3.5 mA (rms) leakage current limit. As can be observed in Figure A2c, the DPWM offset voltage u_{mn} impacts the CM component of the switch-node voltages $\frac{1}{3}(u_{\bar{a}n} + u_{\bar{b}n} + u_{\bar{c}n})$ which now shows a time-varying envelope. However, the offset voltage does not alter the generated DM voltage components relevant for the three-phase output voltage and current formation which are identical to Figure A1d. As illustrated in Figure A2d for phase *a*, the power transistor currents $i_{sa}, i_{s'a}$ remain pulsed in the clamping interval where both s_a and s'_a are permanently turned on. This is a direct consequence of Kirchhoff's current law in the grid *m* and the input stage starpoint *n* as illustrated in Figure A2e where the switching operation of the remaining two phases *b*, *c* defines the high-frequency current flow in the clamped power transistors of phase *a*.