Power Electronic Systems
Laboratory

IEEE Transactions on Transportation Electrification (Early Access)

Non-Isolated Bidirectional Three-Phase Three-Level Wide-Output-Voltage-Range Voltage DC-Link EV Charger

D. Zhang,
J. Kaufmann,
J. Huber,
M. Kasper,
G. Deboy,
J. W. Kolar

ETH zürich

Non-Isolated Bidirectional Three-Phase Three-Level Wide-Output-Voltage-Range Voltage DC-Link EV Charger

Daifei Zhang, Jérome Kaufmann, Jonas Huber, Matthias Kasper, Gerald Deboy, and Johann W. Kolar

***Abstract*—Non-isolated three-phase AC/DC EV chargers show improved efficiency and power density compared to their counterparts with a galvanic isolation stage, but residual current devices (RCDs) are mandatory to ensure electrical safety. However, RCDs are prone to nuisance tripping caused by low-frequency (LF) common-mode (CM) leakage currents through the ground, which therefore must be suppressed. Therefore, first, modulation schemes that do not result in LF CM voltages (i.e., do not employ third harmonic voltage injection) that could drive LF CM currents through parasitic capacitors from the DC output to ground must be employed. Second, closed-loop ground current control (GCC) ensures near-zero LF CM leakage currents even with a direct connection of the charger DC output midpoint to protective earth (PE). Considering a voltage DC-link PFC rectifier system that consists of a boost-type three-level T-type (Vienna) AC/DC-stage and a DC/DC-stage with two stacked buck converters, this paper proposes a new modulation scheme for buck-mode operation at low DC output voltages: the DC/DC-stage then shapes the DC-link voltage such that only one of the AC/DC-stage's three bridge-legs operates with high-frequency switching (1/3-PWM) at any given time, and, different from previous methods, does not require third-harmonic injection to do so. Further, a synergetic GCC is proposed, which operates the two converter stages in the loss-optimum mode for any output DC voltage (buck-mode and boost-mode) and regulates the LF CM ground current to near zero. The proposed concepts are verified using a 10 kW hardware demonstrator with a wide output voltage range (200 V to 800 V) and a direct connection of the DC output midpoint to PE, considering TT (Terra-Terra) and TN (Terra-Neutral) grid grounding systems, whereby the proposed GCC results in LF CM leakage currents below 7 mA, i.e., far below typical RCD trip limits (30 mA). The test voltages obtained with the human-body impedance model from UL 2202 are below 120 mV, i.e., below 50 % of even the most stringent limit of 250 mV of the standard.**

I. Introduction

TRANSPORTATION of both passengers and freight accounts for approximately 25% of the overall global energy consumption [1] and the transportation sector also contributes a significant 25% of the global CO_2 emissions [2]. Through the implementation of enhanced energy conversion technologies and the facilitation of renewable energy integration, electrified transportation thus emerges as a highly promising avenue for substantial mitigation of fossil fuel use and greenhouse gas emissions, but still requires a substantial growth of the electric vehicle (EV) battery charging infrastructure [3].

Recently, extensive research has been carried out on non-isolated chargers for EVs to avoid bulky power processing stages providing galvanic isolation, which also limit the achievable efficiency [4]–[18]. Furthermore, the prevalence of transformerless inverter systems for photovoltaics (PV) can justify the momentum of non-isolated EV chargers: An efficiency improvement of $1\,\% - 2\,\%$ and about twice the power density is identified for transformerless PV inverter systems compared to their galvanically isolated counterparts [19], [20]. In state-of-the-art EV chargers, the galvanic isolation is commonly achieved by a low-frequency transformer or an isolated DC/DC-stage with a high-frequency transformer; both options insert a large common-mode (CM) impedance between the grid and the vehicle that limits the ground current and ultimately ensures electrical safety [21]–[34]. Without galvanic isolation, the non-isolated EV chargers feature improved power conversion efficiencies and/or higher power densities but rely on residual current devices (RCDs)[1] to provide reliable protection against electrical hazards, which are thus mandatory according to relevant standards (e.g., IEC 61851, UL 2202). In the absence of a large CM impedance, excessive ground currents might occur and lead to nuisance tripping of RCDs, which is a main concern regarding non-isolated EV charging systems [4], [9].

Existing literature addresses the suppression of critical ground currents through the implementation of corresponding (passive or active) CM filters. These filters must offer the necessary attenuation not only in the high-frequency (HF) range, such as electromagnetic interference (EMI) measurement frequencies above $150\,\mathrm{kHz}$, but also in the low-frequency (LF) range monitored by residual current devices (RCDs), i.e., below $1\,\mathrm{kHz}$ [9], [11], [13], [14], [16]. An integrated CM filter referenced to the DC-link has proven effective in restricting ground currents [11], [36]–[39]. Furthermore, researchers have proposed various modulation schemes to reduce CM noise emissions. Some focus solely on HF CM noise components [15], while others target both zero LF and HF CM noise in systems with a neutral conductor (three-phase, four-wire systems) [12], [40], [41]. However, while open-loop concepts have been extensively analyzed, closed-loop approaches could potentially prove more reliable.

Therefore, a closed-loop ground current control (GCC) has been proposed by the authors to effectively suppress ground currents and thus avoid nuisance tripping of RCDs [17], [35]: the LF CM ground current (i.e., the sum of the three mains phase currents, which is monitored by RCDs) is measured and regulated to near zero. Specifically, [17] implements the ground current control in a buck-boost *current* DC-link topol-

[1]RCDs are also termed ground fault circuit interrupters (GFCIs).

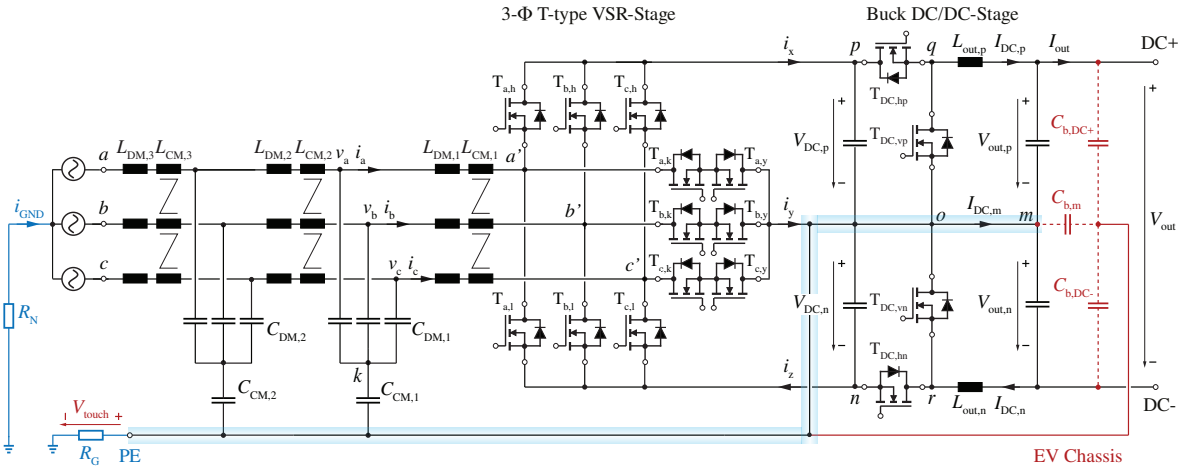

Fig. 1: Power circuit of the considered non-isolated 10 kW three-phase (3-Φ) boost-buck (Bb) voltage DC-link EV charger including CM and DM EMI filters, which employs a 3-Φ three-level (3-L) T-type (Vienna) VSR-stage cascaded by two stacked buck-type DC/DC-stages to cover a wide output voltage of 200 V to 800 V. Employing zero-LF-CM (ZCM) modulation schemes, i.e., 3/3-PWM-ZCM (all three VSR-stage bridge-legs are operating with switching frequency) from [35] in the boost-mode and the newly proposed 1/3-PWM-ZCM (only one of the three VSR-stage bridge-legs is operating with switching frequency) in the buck-mode, facilitates a direct connection of the DC output midpoint m to protective earth (PE), whereby the proposed ground-current control (GCC) regulates the LF ground current $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ to values well below 30 mA, thus preventing nuisance tripping of RCDs. Two grid grounding schemes are considered: TN (Terra-Neutral) with $R_{\mathrm{N}} = R_{\mathrm{G}} = 0\,\Omega$ and TT (Terra-Terra) with $R_{\mathrm{N}} = 10\,\Omega$ and $R_{\mathrm{G}} = 100\,\Omega$ (details see **Section IV-B**). Note further that parasitic capacitances from DC output terminals (and the connected battery pack) to the EV chassis are highlighted in red.

ogy, where a DC-link inductor connects a three-phase buck-type current source AC/DC converter stage (current source rectifier, CSR) and a boost-type DC/DC-stage to cover a wide output voltage range of 300 V to 1000 V as typically required from a universal off-board EV battery charger [42]. The CSR interfaces the 3-Φ mains and realizes ohmic mains behavior with sinusoidal input currents by pulse-width modulating the DC-link current, i.e., distributing the DC-link current to the grid phases. However, all typical PWM methods for current-source AC/DC converters create LF CM voltage components as byproducts. Thus, the GCC proposed in [17] utilizes the DC/DC-stage to actively inject a compensating LF CM voltage to ensure a near-zero CM (ZCM) voltage at the midpoint of the DC output.[2] The DC output midpoint can then be connected to protective earth (PE) since the GCC ensures a closed-loop regulation of the ground current to essentially zero.

Differently, [35] implements GCC in a boost-type 3-Φ T-type voltage-source rectifier (VSR-stage shown in **Fig. 1**). There, sinusoidal PWM without third-harmonic injection can be employed such that no LF CM voltage is generated (see **Fig. 2a**). Note that this is intrinsically different from the current DC-link system [42] discussed above, where the AC/DC stage always generates an LF CM voltage that must be actively canceled by another converter stage.

To again provide a wide output voltage range of 200 V to 800 V, the 3-Φ T-type VSR-stage is extended by a cascaded 3-L buck-type DC/DC-stage for universal EV charger applications in [44], resulting in a topology similar to that shown in **Fig. 1** but without the connection between nodes o, m, and protective earth (PE). In the boost-mode operation, i.e., for high output DC voltages, the 3-Φ three-level bridge-legs of the VSR-stage are continuously pulse-width modulated to regulate the output voltage and the DC/DC-stage remains clamped (i.e., transistors $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently turned on) to avoid switching losses. In the buck-mode operation, i.e., for low output DC voltages, where the output voltage needs to be stepped down from the 3-Φ mains, the DC/DC-stage must be activated, too. An advanced 1/3-PWM scheme is applied to significantly reduce the switching losses of the 3-Φ T-type PFC rectifier front-end [43]: The 1/3-PWM scheme, first proposed in early 2000 for a 2-L voltage-source converter [45]–[47], requires the DC/DC-stage to create a time-varying six-pulse-shaped DC-link voltage $V_{\mathrm{DC}} = v_{\mathrm{pn}}$, which allows to clamp two phases of the VSR-stage and to operate only one remaining phase with PWM hence the name "1/3-PWM".

However, the topology from [44] cannot be directly applied as a non-isolated EV charger since a direct connection to the protective earth (PE) is impossible due to the LF CM voltage used in the modulation schemes, and, ultimately, the ground current control cannot be achieved to avoid the nuisance tripping of the RCDs. So far, it has not been shown how both 1/3-PWM *and* ground current control can be applied to allow the non-isolated EV charger operation. This paper fills the research gap by first conducting the necessary hardware modification, i.e., introducing a direct connection (see the highlighted connection in **Fig. 1**) between the protective earth (PE), the DC-link midpoint o, and the output midpoint m, to form a low-impedance path for the ground current. The hardware change also poses an additional constraint on the implemented PWM schemes, i.e., no LF CM voltage is allowed to be injected by the AC/DC-stage. Otherwise, a considerable LF CM current would flow since a low-impedance CM current path is intentionally created.

In principle, GCC with 3/3-PWM-ZCM (see **Fig. 2a**) could

[2]It is important to highlight that [17] presents a *current DC-link* topology, requiring that the DC/DC-stage actively injects an LF CM voltage to compensate the LF CM voltage inevitably generated by the AC/DC-stage in order to avoid the nuisance tripping of the RCD. In contrast, this paper investigates the *voltage DC-link* converter shwon in **Fig. 1**, where the AC/DC-stage can operate with zero LF CM voltage injection over the wide output voltage range by using proper ZCM modulation schemes.

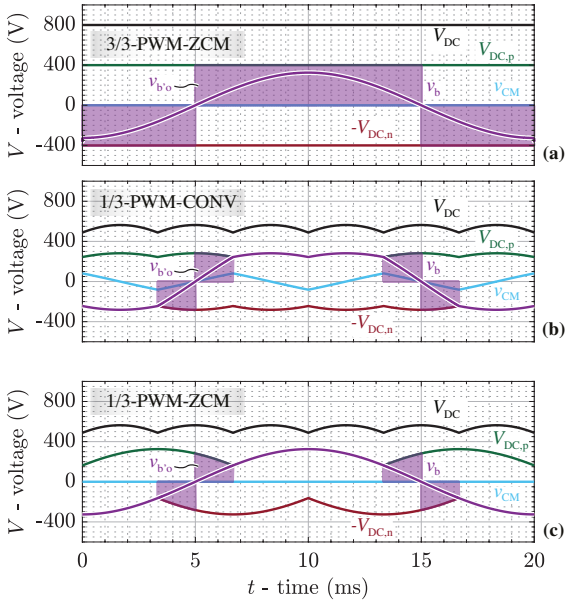

Fig. 2: Conceptual key waveforms of different pulse-width modulation (PWM) schemes in the context of the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1**. **(a)** 3/3-PWM-ZCM operation for the VSR-stage with a constant DC-link voltage V_{DC} and zero LF CM injection (i.e., sinusoidal PWM without third-harmonic injection), i.e., $v_{CM} = v_{mPE} = v_{oPE} = 0$ [35]. **(b)** Buck-mode operation with active DC/DC-stage that is utilized to shape the DC-link voltage such that always only one out of the three bridge-legs of the AC/DC-stage operates with HF switching [43], [44]; conventionally, an LF CM voltage results. Thus, a direct grounding of the output midpoint m as shown in **Fig. 1** is not possible when applying the conventional 1/3-PWM-CONV. **(c)** Buck-mode operation with the *proposed* 1/3-PWM-ZCM method that retains the overall six-pulse shape of the DC-link voltage from 1/3-PWM-CONV and hence also the loss reduction of the VSR-stage, but allows the zero-LF-CM operation, i.e., compatible with a direct grounding of the DC-output midpoint and thus the proposed GCC.

be implemented for the whole output voltage range. This needs all three-phase bridge-legs continuously switching [35]. However, the DC/DC-stage has to be operated as well in the buck-mode operation to step a high DC-link voltage down to a low DC output voltage, which would lead to high power losses. Instead, in buck-mode operation, the use of 1/3-PWM is preferred to achieve a significant reduction of switching losses. However, the conventional (CONV) 1/3-PWM method [43], [44] leads again to the formation of an LF CM voltage as shown in **Fig. 2b** and therefore is not compatible with grounding the DC output midpoint as desired for non-isolated EV chargers (see **Fig. 1**). There is, thus, a need for a new modulation scheme that allows to advantageously maintain the low losses of 1/3-PWM while at the same time enabling operation as a non-isolated EV charger, i.e., with zero CM injection.

Therefore, this paper first proposes a new 1/3-PWM-ZCM scheme with zero LF CM voltage generation for the topology shown in **Fig. 1**, which is achieved by breaking the conventionally [43], [44] employed equality constraint $V_{DC,p} = V_{DC,n}$ between the upper and the lower DC-link voltages, respectively (see **Fig. 2c**). This still allows maintaining the six-pulse shape of the overall DC-link voltage V_{DC} and hence the switching loss reduction for the AC/DC-stage by clamping two out of three phases. However, to independently control $V_{DC,p}$ and $V_{DC,n}$, the DC/DC-stage is realized by two stacked buck converters, and a direct connection between the DC-link midpoint o and the output midpoint m is thus needed. Further, the absence of LF CM voltages enables a direct connection of the output midpoint m to PE (see the highlighted connection in **Fig. 1**), whereby the proposed GCC ensures near-zero ground current.

Furthermore, as derived in detail in **Section II**, combining the proposed 1/3-PWM-ZCM and the 3/3-PWM-ZCM from [35] achieves loss-optimum operation of the non-isolated 3-Φ boost-buck (Bb) voltage DC-link EV charger (see **Fig. 1**) over the full output voltage range. Then, a new synergetic control concept is introduced in **Section III**, which ensures seamless transitions between different loss-optimum operating modes (at different output voltage levels) while closed-loop-controlling the LF CM ground current to near zero. **Section IV** presents a comprehensive experimental verification of the novel modulation and control concept using a 10 kW hardware demonstrator, and, considering a wide output voltage and power range, demonstrates LF CM leakage currents below 7 mA rms for a direct connection of the output midpoint to PE, i.e., well below typical RCD trip levels of 30 mA. Similarly, employing the human-body impedance model according to UL 2202 results in test voltages below 120 mV, i.e., well below the most strict limit of 250 mV given in the standard. Finally, **Section V** concludes this paper.

II. Operating Principle

This section focuses on the operating principle of the analyzed non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1**, considering a 400 V rms line-to-line mains with near-unity power factor, and a wide output voltage range of 200 V to 800 V. Targeting non-isolated EV charger applications that require RCDs at the AC input to ensure electrical safety, zero-LF-CM PWM schemes must be applied to enable a direct low-impedance connection between the DC-link midpoint m and protective earth (PE). Then, the ground current i_{GND} can be measured and actively regulated to near zero (see **Section III**), avoiding the nuisance tripping of the RCDs. Further, the loss-optimal operation of the two-stage system requires that both the VSR-stage and the DC/DC-stage operate with the minimum possible DC-link voltage and with the minimum number of HF-switching half-bridges (HBs), i.e., three out of five HBs[3], which ensures minimum overall switching losses.

Both aims are achieved by combining the 3/3-PWM-ZCM and the proposed 1/3-PWM-ZCM, which can be derived from very generic voltage transfer limitations of the VSR-stage and the DC/DC-stage. The limits for the VSR-stage have been derived based on Kirchhoff's Voltage Law in [44], where equal upper and lower DC-link voltages, i.e., $V_{DC,p} = V_{DC,n} =$

[3]Note, first, that each of the VSR-stage's 3-L bridge-legs effectively consist of two HBs each; however, only one out of the two is active at any given time, depending on the polarity of the switch-node voltage reference to be generated. Therefore, a total of five HBs (three VSR-stage and two DC/DC-stage HBs) *could* be HF-switching in total, but as only three degrees of freedom must be controlled, i.e., two mains currents for PFC operation with a desired power flow and the ground current (or the third mains current) for electrical safety, only a minimum of three HBs *mus*t operate with HF switching.

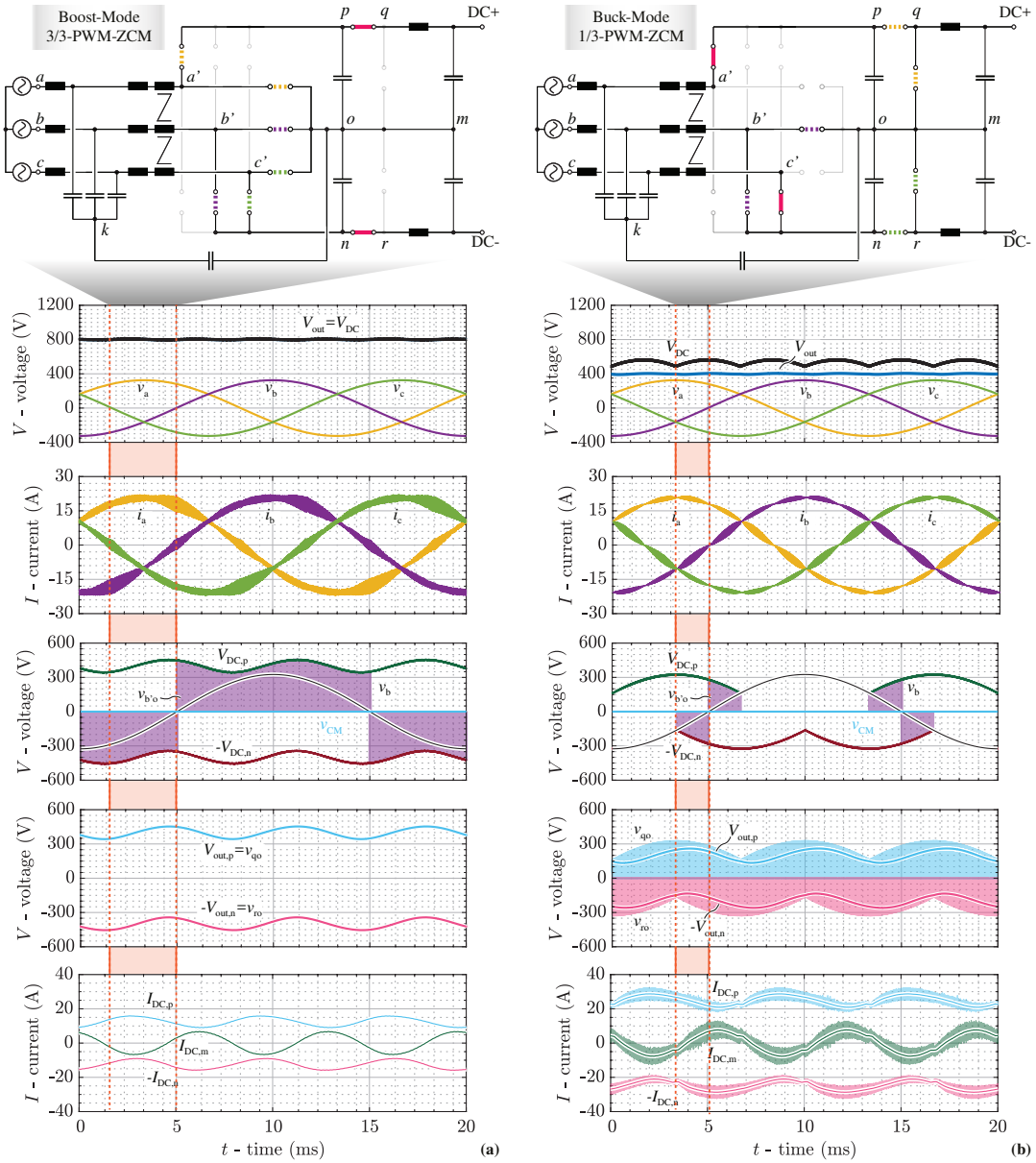

Fig. 3: Circuit states of the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1** during the highlighted part of the mains period, when operating with **(a)** 3/3-PWM-ZCM and **(b)** 1/3-PWM-ZCM: dashed lines indicates a HF-switching transistor whereas solid lines indicate permanently turned-on transistors. Simulated key waveforms include the phase-b switched voltage of the VSR-stage, $v_{\mathrm{b'o}}$, which indicates the VSR-stage modulation method (with 1/3-PWM-ZCM, $v_{\mathrm{b'o}}$ shows HF switching for only one third of a mains period, because the DC/DC-stage shapes the DC-link voltages to follow the minimum and maximum phase voltage, respectively). The switched output voltages, v_{qo} and v_{ro}, indicate the HF-switching or the clamping states of the DC/DC-stage HBs. Note that the DC-link and the output voltages are, in general, asymmetric, i.e., $V_{\mathrm{DC,p}} \neq V_{\mathrm{DC,n}}$ and $V_{\mathrm{out,p}} \neq V_{\mathrm{out,n}}$ for both ZCM modulation methods, whereas the total output voltage $V_{\mathrm{out}} = V_{\mathrm{out,p}} + V_{\mathrm{out,n}}$ is always constant.

$V_{\mathrm{DC}}/2$, have been assumed; breaking this equality restriction yields

$$-V_{\mathrm{DC,n}} = V_{\mathrm{no}} \leq \bar{v}_{\mathrm{s'k}} + v_{\mathrm{CM}} \leq V_{\mathrm{po}} = V_{\mathrm{DC,p}}, \qquad (1)$$

where $\mathrm{s} \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ and $\bar{v}_{\mathrm{s'k}}$ is the local average (over one switching period) DM voltage at the VSR-stage switching node with reference to the artificial neutral point k. This requirement must be fulfilled by all three phases, respectively, and the total DC-link voltage is $V_{\mathrm{DC}} = V_{\mathrm{DC,p}} + V_{\mathrm{DC,n}}$. Note that $v_{\mathrm{CM}} = 0$ should be achieved such that the artificial neutral point k (equivalent to PE under 3-Φ symmetric mains) is at a potential close to the output midpoint m. This, then, allows a low impedance connection between PE and m such that the GCC can be applied to ensure a zero LF CM ground current as needed by non-isolated EV chargers [17], [35]. Furthermore, the DC/DC-stage is limited to buck-type (step-down) behavior for the upper and lower HBs, i.e.,

$$V_{\mathrm{out,p}} = \bar{v}_{\mathrm{qo}} \leq V_{\mathrm{DC,p}} \quad \text{and} \quad V_{\mathrm{out,n}} = \bar{v}_{\mathrm{or}} \leq V_{\mathrm{DC,n}}. \qquad (2)$$

The requirements in (1) and (2) must be met simultaneously to ensure a constant power delivery, i.e., to draw 3-Φ sinusoidal mains currents and to generate a constant DC output voltage. Combining the constraints for the VSR-stage and the DC/DC-

TABLE I: Specifications and key components of the realized non-isolated 3-Φ Bb voltage DC-link EV charger in **Fig. 1**.

	Description	Value
V_{in}	Rms phase voltage	230 V
V_{out}	DC output voltage range	200 V ∼ 800 V
P_{out}	Rated output power	10 kW
$I_{\text{out,max}}$	Output current limit	25 A ($V_{\text{out}} < 400$ V)
T_{VSR}	VSR-stage semicond. $\text{T}_{\text{h\{1\}}}$	C3M0016120K, 1200 V, 16 mΩ
	VSR-stage semicond. $\text{T}_{\text{k\{y\}}}$	C3M0030090K, 900 V, 30 mΩ
f_{VSR}	VSR-stage sw. freq.	100 kHz
$\text{T}_{\text{DC/DC}}$	DC/DC-stage semicond.	C3M0010090K, 900 V, 10 mΩ
$f_{\text{DC/DC}}$	DC/DC-stage sw. freq.	200 kHz
C_{DC}	DC-link cap.	2×6.6 µF
C_{out}	Output cap.	2×65 µF
$L_{\text{DM,1}}$	Main input DM ind.	3×194 µH (2×KoolMu60 E43/17, 25 turns)
$L_{\text{CM,1}}$	Main input CM ind.	4.6 mH (2×VAC 45/30/15, 12 turns)
L_{out}	Output DM ind.	2×96 µH (3×N87 E47/20/16, 12 turns)
$C_{\text{DM,1}}$	1st EMI DM capacitor	3×3 µF
$C_{\text{CM,1}}$	1st EMI CM capacitor	40 nF
$L_{\text{DM,2}}$	2nd EMI DM inductor	3×15 µH, *WE 7443641500*
$C_{\text{DM,2}}$	2nd EMI DM capacitor	3×6 µF
$L_{\text{CM,2}}$	2nd EMI CM inductor	870 µH, VAC 25/16/10, 8 turns
$C_{\text{CM,2}}$	2nd EMI CM capacitor	18 nF
$L_{\text{DM,3}}$	3rd EMI DM inductor	3×4.7 µH, *WE 7443640470*
$L_{\text{CM,3}}$	3rd EMI DM inductor	870 µH, VAC 25/16/10, 8 turns

stage leads to

$$\max(v_{\text{max}}, V_{\text{out,p}}) \leq V_{\text{DC,p}} \quad \text{and} \tag{3}$$

$$\max(-v_{\text{min}}, V_{\text{out,n}}) \leq V_{\text{DC,n}}, \tag{4}$$

where $v_{\text{max}} = \max(\bar{v}_{\text{s'k}})$ and $v_{\text{min}} = \min(\bar{v}_{\text{s'k}})$ are the maximum and the minimum local average DM voltages at the VSR-stage switching node, respectively. Importantly, to minimize the number of HF-switching HBs and hence the switching losses, the equalities in (3) and (4) are preferably met at any time regardless of the output voltage. This then directly results in the proposed different operating modes and PWM schemes of the VSR-stage for different parts of the wide output voltage range, as described in the following.

Specifically, two main modulation schemes, i.e., 3/3-PWM-ZCM and 1/3-PWM-ZCM (see **Fig. 3**), cover the wide output voltage range, which is divided into three operating modes, i.e., boost-, buck-, and transition-mode. Note that with ZCM modulation schemes, the DC-link capacitor voltages, $V_{\text{DC,p}}$ and $V_{\text{DC,n}}$, and the output capacitor voltages, $V_{\text{out,p}}$ and $V_{\text{out,n}}$, are not constant but time-varying (note that the constant value of the output terminal voltage $V_{\text{out}} = V_{\text{out,p}} + V_{\text{out,n}}$ is still maintained). Furthermore, the amplitudes of these voltage variations depend on the output power, the DC-link capacitance, and the output capacitance. As a result, the dividing lines between different modes also depend on these factors; for the rest of this paper, therefore, the specifications and the component values (see **Tab. I**) of the realized hardware prototype are considered.

A. Boost-Mode and 3/3-PWM-ZCM ($V_{\text{out}} > 670$ V)

In cases where the output voltages are high enough such that

$$v_{\text{max}} \leq V_{\text{out,p}} = V_{\text{DC,p}} \quad \text{and} \tag{5}$$

$$-v_{\text{min}} \leq V_{\text{out,n}} = V_{\text{DC,n}}, \tag{6}$$

the converter operates in the boost-mode (see **Fig. 3a**): the VSR-stage uses 3/3-PWM-ZCM, where all three bridge-legs of the VSR-stage operate with HF PWM to ensure 3-Φ sinusoidal mains currents and step up the 3-Φ mains voltages to the higher DC output voltage, i.e., $V_{\text{DC}} = V_{\text{out}}$. The two HBs of the DC/DC-stage are both clamped, i.e., the switches $\text{T}_{\text{DC,hp}}$ and $\text{T}_{\text{DC,hn}}$ of the DC/DC-stage are permanently on and do not contribute to switching losses.

Fig. 3a also presents the simulated characteristic waveforms in the boost-mode operation, where each of the VSR-stage's three bridge-legs (phase *b* is shown in the figure as an example) operates with HF switching over the entire mains period, but both DC/DC-stage HBs are permanently clamped. However, an LF current $I_{\text{DC,m}}$ with a rms value of 6 A flowing between the DC-link midpoint *o* and the output midpoint m is observed. $I_{\text{DC,m}}$ closes its path through the upper and lower DC/DC-stage inductors, and thus LF variations occur in the $I_{\text{DC,p}}$ and $I_{\text{DC,n}}$ as well. However, this contributes to additional conduction losses of the DC/DC-stage to a limited extent only (see detailed analysis in **Section IV-C**). Similarly, an LF (150 Hz) variation of the DC-link capacitor voltages, $V_{\text{DC,p}}$ and $V_{\text{DC,n}}$, and of the output capacitor voltages, $V_{\text{out,p}}$ and $V_{\text{out,n}}$, can be observed. This variation must be taken into account regarding the blocking voltage rating of the transistors, but can be lowered by increasing the capacitance values.

Most importantly, the DC output midpoint does not exhibit any CM voltage ($v_{\text{cm}} = 0$). Nevertheless, the LF variation of the output capacitor voltages still could drive a current through the parasitic capacitances $C_{\text{b,DC+}}$ and $C_{\text{b,DC-}}$ to the EV chassis (see **Fig. 1**). While the majority of this current closes its path through the local DC-link midpoint due to relatively low impedance, a small portion of the current might find its way through PE and 3-Φ mains terminals, potentially tripping the RCD. Therefore, closed-loop control of the ground current as introduced below in **Section III** is needed to reliably prevent nuisance tripping of the RCD (see also **Section IV-A** for further discussion). Finally, it's worth noting that 3-Φ sinusoidal currents and constant DC output voltage V_{out} are generated regardless of the asymmetry of the two DC-link voltages.

B. Buck-Mode and Proposed 1/3-PWM-ZCM ($V_{\text{out}} < 430$ V)

In cases where the output voltages are low such that

$$V_{\text{out,p}} \leq v_{\text{max}} = V_{\text{DC,p}} \quad \text{and} \tag{7}$$

$$V_{\text{out,n}} \leq -v_{\text{min}} = V_{\text{DC,n}}, \tag{8}$$

the converter operates in the buck-mode (see **Fig. 3b**): For such low output voltages, the DC/DC-stage *must* operate to step down the upper/lower DC-link voltages to the corresponding required upper/lower output voltages. Advantageously, the

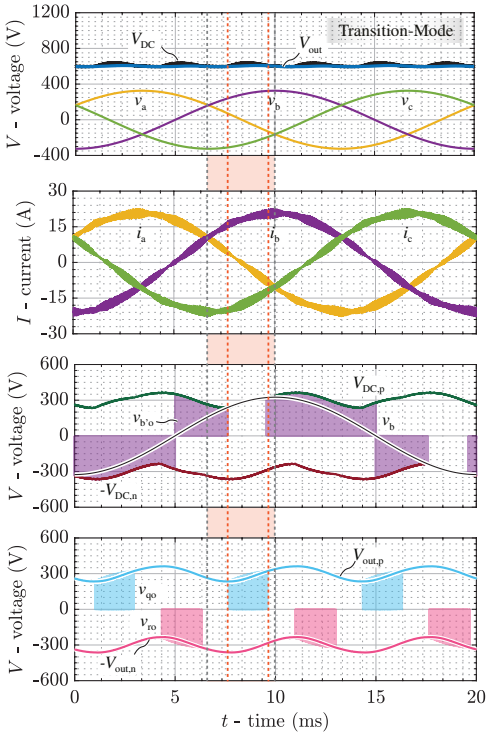

Fig. 4: Simulated key waveforms of the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1** when operating in the transition-mode. One 60°-sector of one mains period ($v_b > v_a > v_c$) is highlighted with a shaded background; note that the converter operates with 1/3-PWM-ZCM in a part of this sector (where the DC/DC-stage's upper HB is HF-switching, delineated by the dashed orange lines) and with 3/3-PWM-ZCM otherwise.

DC/DC-stage shapes the total DC-link voltage V_{DC} to follow the six-pulse shape of the envelope of the 3-Φ line-to-line mains voltage absolute values to facilitate 1/3-PWM operation of the VSR-stage.

Different from the conventional 1/3-PWM-CONV from [43], [44], however, the upper and lower DC-link voltages are shaped *individually*: The upper (lower) DC/DC-stage HB regulates the upper (lower) DC-link voltage to v_{max} ($-v_{min}$) to achieve 1/3-PWM operation of the VSR-stage without any CM injection. Then, the VSR-stage uses 1/3-PWM-ZCM, where at any given point in time, only one of the VSR-stage's three bridge-legs operates with HF PWM such that a considerable switching loss reduction is achieved. This results again (as for 3/3-PWM-ZCM discussed above) in an LF current $I_{DC,m}$ that flows through the output capacitors and the DC/DC-stage inductors and also in LF variations of the output capacitor voltages, but nevertheless a constant DC output voltage V_{out} is achieved.

C. Transition-Mode ($430\,\mathrm{V} < V_{out} < 670\,\mathrm{V}$)

The 3-Φ mains voltages, v_{max} and v_{min}, and the output capacitor voltages, $V_{out,p}$ and $V_{out,n}$, are time-varying over one mains period (see **Fig. 3**). Thus, it is possible that v_{max} and $V_{out,p}$ are alternatively equal to the upper DC-link voltage $V_{DC,p}$ during one mains period according to (3). The same situation occurs for the lower half of the system: $-v_{min}$ and $V_{out,n}$ are alternatively equal to the lower DC-link voltage $V_{DC,n}$ during one mains period according to (4). To facilitate the explanation, one 3-Φ mains 60°-sector where $v_b > v_a > v_c$ is highlighted (shaded area) in **Fig. 4**, which shows simulated key waveforms: During the time interval between the two dashed lines, $V_{DC,p} = v_{max} \geq V_{out,p}$ such that the VSR-stage's phase-b bridge-leg is clamped to the positive DC-rail and the upper DC/DC-stage HB operates with HF-switching to step down the upper DC-link voltage $V_{DC,p}$ to the uper output voltage $V_{out,p}$.

However, different from the buck-mode, the lower DC/DC-stage HB does *not* operate with HF-switching but actually is clamped since $V_{DC,n} = V_{out,n} \geq -v_{min}$. Thus, in total, two of the VSR-stage's bridge-legs and one of the DC/DC-stage's two HBs are switching, i.e., three HB's in total, such that the minimum number of HF-switching HBs is still guaranteed. During the rest of the time in this sector, the converter operates like in the boost-mode where both upper and lower DC/DC-stage HBs are clamped and the VSR-stage operates with 3/3-PWM-ZCM, i.e., again with a total of three HF-switching HBs. Note that the phase shift between v_{max} and v_{min} leads to a phase-shifted activation of the DC/DC-stage HBs, but the 60°-sector symmetry over one mains period is still maintained such that the analysis of a single sector remains representative.

Thus, the transition mode fills the gap between the buck mode and the boost mode, such that loss-optimum ZCM modulation schemes exist for the entire wide output voltage range.

III. Synergetic Control Strategy

The proposed synergetic control strategy shown in **Fig. 5** is based on the conventional synergetic control method from [44] but includes the proposed ground current control (GCC), i.e., ensures a synergetic/collaborative operation of the VSR-stage and the two DC/DC-stage HBs such that the non-isolated EV charger operates in the loss-optimum mode with zero CM injection for any operating point. Furthermore, automatic and seamless transitions between the operating modes, i.e., boost or buck operation in case of changing operating points, are guaranteed. The control system is explained in detail in the following subsections. Furthermore, the controller design is provided in **Appendix A**, and the proposed control strategy can also cope with irregular mains conditions, as is briefly discussed in the **Appendix B**.

A. Output Voltage Control & Mains Current Control

The output voltage regulation loop tracks the reference V_{out}^* by supplying the required power reference P_{out}^* and, equivalently, the VSR-stage's input conductance reference G^*. The 3-Φ mains current references i_a^*, i_b^*, and i_c^*, are proportional to the measured 3-Φ input voltages v_a, v_b, and v_c, ensuring purely ohmic mains behavior.

The mains current errors, resulting from the difference between the references and the measured 3-Φ boost inductor currents, are fed into the mains current controller to derive the required 3-Φ boost inductor voltages v_{La}^*, v_{Lb}^*, and v_{Lc}^*, required for impressing the desired phase currents.

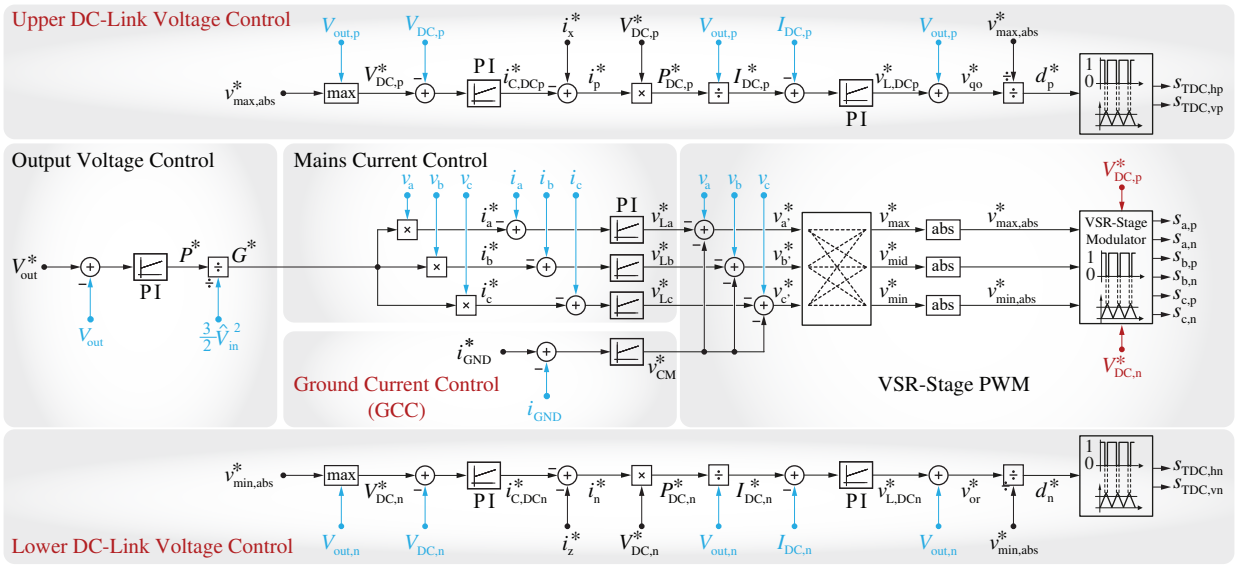

Fig. 5: Proposed control block diagram for the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1**. It is based on the synergetic control concept from [44] but, in addition, newly-implemented blocks for the proposed zero-LF-CM modulation schemes (3/3-PWM-ZCM and proposed 1/3-PWM-ZCM) and closed-loop ground current control (GCC) are highlighted in red. The functionality and the interaction of the individual control blocks are described in **Section III**. Note that all quantities refer to local average values here.

B. Ground Current Control (GCC)

A direct feedback control of the LF CM ground *current* is the most reliable way to prevent nuisance tripping of RCDs [17]. Such a ground current control of the 3-Φ 3-L T-type rectifier using 3/3-PWM-ZCM has been proposed in [35], where a CM control voltage is injected to regulate the ground current i_{GND} (see **Fig. 1**). It has also been proven that DM and CM components can be independently regulated, i.e., regulating the ground current (a CM quantity) has a negligible impact on the generation of the 3-Φ sinusoidal mains currents and the DC output voltage (DM quantities). Considering 1/3-PWM-ZCM and 3/3-PWM-ZCM are only different in the DM behavior, both have no CM injection. Thus, a similar ground current control strategy can be applied in the analyzed 3-Φ non-isolated EV charger to achieve near-zero ground current for both 1/3-PWM-ZCM and 3/3-PWM-ZCM.

Therefore, the sum of the 3-Φ mains phase currents, i.e., $i_{\mathrm{GND}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}}$ as shown in **Fig. 1**, is measured (the same measurement method is implemented in RCDs), and then compared to the ground current reference i^*_{GND} with $i^*_{\mathrm{GND}} = 0\,\mathrm{A}$ in most cases, to calculate the ground current error. The error is forwarded into the ground current controller to derive the required LF CM correction voltage v^*_{CM}. For the sake of brevity, the PI controller tuning, based on [35], is not further detailed here.

C. VSR-Stage PWM

Subtracting the calculated inductor voltage references v^*_{La}, v^*_{Lb}, and v^*_{Lc} from the measured 3-Φ input voltages (mains voltage feedforward) results in the DM components of the VSR-stage's switch-node voltages. Then, the LF CM voltage reference v^*_{CM} obtained from the GCC is added to obtain the 3-Φ VSR-stage voltage references v^*_{a}, v^*_{b}, and v^*_{c}. These voltage references and the corresponding upper and lower DC-link voltage references $V^*_{\mathrm{DC,p}}$ and $V^*_{\mathrm{DC,n}}$ (see **Section III-D** below) then define the 3-Φ duty cycles, e.g., considering phase *a*, as:

$$d^*_{\mathrm{a}} = \begin{cases} v^*_{\mathrm{a}}/V^*_{\mathrm{DC,n}} & v^*_{\mathrm{a}} \le 0 \\ v^*_{\mathrm{a}}/V^*_{\mathrm{DC,p}} & v^*_{\mathrm{a}} > 0 \end{cases}. \tag{9}$$

Furthermore, it is important to highlight that due to asymmetric DC-link capacitor voltages, either the upper or the lower DC-link capacitor voltage is assigned to calculate the duty cycles according to the polarity of the phase voltage reference.

D. Upper/Lower DC-Link Voltage Control

The selection of appropriate upper and lower DC-link voltage references $V^*_{\mathrm{DC,p}}$ and $V^*_{\mathrm{DC,n}}$ is at the core of the proposed synergetic control structure with zero LF CM voltage injection and GCC, and vital to achieving seamless and automatic transitions between the different operating modes and modulation schemes. Based on (3) and (4), the two voltage references are defined as

$$V^*_{\mathrm{DC,p}} = \max(v^*_{\mathrm{max,abs}}, V_{\mathrm{out,p}}) \quad \text{and} \tag{10}$$

$$V^*_{\mathrm{DC,n}} = \max(v^*_{\mathrm{min,abs}}, V_{\mathrm{out,n}}). \tag{11}$$

This ensures that two HBs out of five are always clamped without generating switching losses, i.e., loss-optimal operation. Both DC-link voltages are closed-loop-controlled by comparing their references with the measured DC-link voltages $V_{\mathrm{DC,p}}$ and $V_{\mathrm{DC,n}}$. The deviations are processed by two PI controllers that then define the required DC-link capacitor currents, $i^*_{\mathrm{C,DCp}}$ and $i^*_{\mathrm{C,DCn}}$, needed to counteract the control error. The LF input current references, i^*_{p} and i^*_{n}, of the two DC/DC-stage HBs further include the feedforwarded currents, i^*_{x} and i^*_{z}, flowing through the VSR-stage's upper/lower DC rails, which can be calculated with the information of the measured 3-Φ boost inductor currents and the calculated 3-Φ duty cycles. Thus,

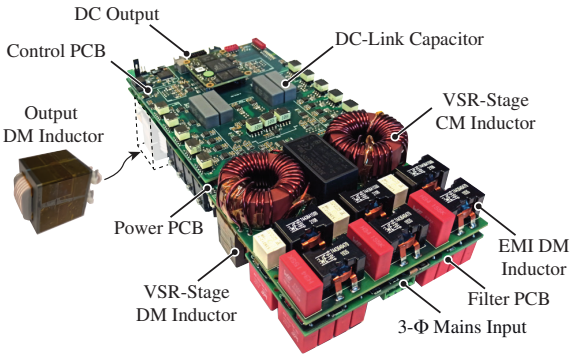

Fig. 6: Photo of the realized non-isolated 3-Φ Bb voltage DC-link EV charger hardware demonstrator (see **Fig. 1** for the schematics and **Tab. I** for key components). Necessary modifications are conducted on the existing converter built in [44], i.e., two new output DM inductors are used in two stacked buck-type DC/DC-stages to replace the previous output DM and CM inductors. This leads to an additional volume of $65\,\mathrm{cm}^3$ and results in a power density of $5.2\,\mathrm{kW/L}$ ($86\,\mathrm{W/in}^3$). Operating from the 400 V 3-Φ mains and employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs, a wide output voltage range of 200 V – 800 V is covered.

the power references $P^*_{\mathrm{DC,p}}$ and $P^*_{\mathrm{DC,n}}$ of these two HBs can be obtained, from which the two DC/DC-stage buck-inductor current references $I^*_{\mathrm{DC,p}}$ and $I^*_{\mathrm{DC,n}}$ follow by dividing with the two output capacitor voltages $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$.

$I^*_{\mathrm{DC,p}}$ and $I^*_{\mathrm{DC,n}}$ are compared with the measured values to determine the respective required inductor voltages $v^*_{\mathrm{L,DCp}}$ and $v^*_{\mathrm{L,DCn}}$. The sum of these inductor voltages and the respective output capacitor voltage (output voltage feedforward) leads to the output voltage references v^*_{qo} and v^*_{or} of the two DC/DC-stage HBs. Then, the two duty cycles are given by

$$d^*_{\mathrm{p}} = \frac{v^*_{\mathrm{qo}}}{v^*_{\mathrm{max,abs}}} = \frac{v^*_{\mathrm{L,DCp}} + V_{\mathrm{out,p}}}{v^*_{\mathrm{max,abs}}}, \quad \text{and} \tag{12}$$

$$d^*_{\mathrm{n}} = \frac{v^*_{\mathrm{or}}}{v^*_{\mathrm{min,abs}}} = \frac{v^*_{\mathrm{L,DCn}} + V_{\mathrm{out,n}}}{v^*_{\mathrm{min,abs}}}. \tag{13}$$

For the boost-mode operation where $V_{\mathrm{out,p}} > v_{\mathrm{max,abs}}$ and $V_{\mathrm{out,n}} > v_{\mathrm{min,abs}}$, d^*_{p} and d^*_{n} are always saturated to the full duty cycles, i.e., the switches $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ of the DC/DC-stage are permanently on, considering comparably small inductor voltages $v^*_{\mathrm{L,DCp}}$ and $v^*_{\mathrm{L,\,DCn}}$. For the AC/DC-stage, the 3-Φ duty cycles calculated using (9) are always smaller than 1 as $V^*_{\mathrm{DC,p}} > v_{\mathrm{max,abs}}$ and $V^*_{\mathrm{DC,n}} > v_{\mathrm{min,abs}}$, and thus, the AC/DC-stage automatically operates with 3/3-PWM-ZCM.

On the other hand, for the buck-mode operation where $V_{\mathrm{out,p}} < v_{\mathrm{max,abs}}$ and $V_{\mathrm{out,n}} < v_{\mathrm{min,abs}}$, the two DC/DC-stage HBs regulate the upper and lower DC-link voltages, and indirectly control the 3-Φ input currents. For the AC/DC-stage whose duty cycles are derived from (9), the phase with the maximum phase voltage is automatically clamped to the positive rail as $V^*_{\mathrm{DC,p}} = v_{\mathrm{max,abs}}$ and the phase with the minimum phase voltage is clamped to the negative rail as $V^*_{\mathrm{DC,n}} = v_{\mathrm{min,abs}}$. Thus, two out of the 3-Φ duty cycles are equal to 1 when operating with 1/3-PWM-ZCM.

Therefore, importantly, seamless transitions between different loss-optimal operating modes and modulation schemes are inherently achieved using the five half-bridge duty cycles calculated in (9) and (12).

IV. Hardware and Experimental Verification

The proposed 1/3-PWM-ZCM and the synergetic GCC have been verified using a $10\,\mathrm{kW}$ hardware demonstrator (see **Fig. 6**) of the non-isolated 3-Φ Bb voltage DC-link EV charger system from **Fig. 1** and **Tab. I** summarizes the key specifications and components. The advanced control strategy is executed on a Zynq 7000 SoC featuring a dual-core ARM Cortex-A9 processor integrated with a $100\,\mathrm{MHz}$ programmable logic fabric.

A. Experimental Waveforms

Fig. 7 shows measured key waveforms of the $10\,\mathrm{kW}$ hardware demonstrator, i.e., phase *a* voltage v_{a}, phase *a* current i_{a}, DC-link voltage V_{DC}, and output voltage V_{out}, to verify the basic converter functionalities. Furthermore, the switched voltage of phase *a*, $v_{\mathrm{a'o}}$, clearly differentiates the HF-switching or clamping states of the corresponding VSR-stage bridge-leg. Likewise, the switched voltage of the DC/DC-stage's upper HB, v_{qo}, indicates the HF-switching and clamping intervals.

Fig. 7a presents the buck-mode operation with $V_{\mathrm{out}} = 200\,\mathrm{V}$ and $P_{\mathrm{out}} = 5\,\mathrm{kW}$. The upper DC/DC-stage HB regulates the upper DC-link voltage $V_{\mathrm{DC,p}}$ to the required three-pulse shape, i.e., the upper envelope of the 3-Φ mains voltages[4]; likewise, the lower DC/DC-stage HB regulates the lower DC-link voltage $V_{\mathrm{DC,n}}$ to the three-pulse shape given by the amplitude of the lower envelope of the 3-Φ mains. Thus, the total DC-link voltage V_{DC} follows the six-pulse shape, i.e., the envelope of the line-to-line voltage absolute values, required to achieve 1/3-PWM-ZCM operation (see $v_{\mathrm{a'y}}$) of the VSR-stage, i.e., each bridge-leg switches during only one third of the mains period, and without generating an LF CM voltage. **Fig. 7c** shows the boost-mode operation with $V_{\mathrm{out}} = 800\,\mathrm{V}$ and $P_{\mathrm{out}} = 10\,\mathrm{kW}$, where all three bridge-legs of the VSR-stage switch continuously at HF and the DC/DC-stage clamps, i.e., $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently on. **Fig. 7b** presents the transition-mode operation with $V_{\mathrm{out}} = 600\,\mathrm{V}$ and $P_{\mathrm{out}} = 10\,\mathrm{kW}$. In all cases, the waveforms are in excellent agreement with the simulation results from **Fig. 3** and **Fig. 4**, respectively.

The proposed synergetic control strategy is further verified in **Fig. 8**, where automatic and smooth transitions between different operating modes are achieved when the output voltage reference increases from 300 V to 700 V. Note that stepping from the buck-mode operation to the boost-mode operation, the HF-switching interval of the VSR-stage phase bridge-leg is gradually extended and the HF-switching interval of the DC/DC-stage HB is shortened until fully clamped in the boost-mode operation. Further, GCC maintains the ground current at essentially zero during the transition.

Note that the DC output voltages $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$, i.e., the voltages of the battery terminals DC+ and DC- with respect to the chassis (see **Fig. 1**) show LF (mainly $150\,\mathrm{Hz}$) voltage variations (see **Fig. 7**). These drive ground (leakage) currents through the parasitic capacitances $C_{\mathrm{b,DC+}}$ and $C_{\mathrm{b,DC-}}$, which are

[4]Note that assuming small voltage drops over the 3-Φ filter inductors (e.g., $L_{\mathrm{DM,1}}$), the mains voltages equal to the local average (over one switching period) switch-node voltages. Thus, in the buck-mode operation, the upper DC-link voltage follows the upper envelope of the 3-Φ mains voltages.

Fig. 7: Experimental waveforms of the converter shown in **Fig. 1** with the proposed synergetic control strategy (see **Fig. 5**) when operating in **(a)** ***buck-mode***, **(b)** ***transition-mode*** and **(c)** ***boost-mode*** in the TN system ($R_G = R_N = 0\,\Omega$ in **Fig. 1**). In the ***buck-mode*** operation, the upper DC/DC-stage regulates the upper DC-link voltage $V_{DC,p}$ to the three-pulse shape (the upper envelope of the 3-Φ mains voltage) to facilitate 1/3-PWM-ZCM of the VSR-stage where only one phase (the phase with minimum voltage amplitude) is HF-switching at any given time (see the switched voltage $v_{a'o}$ of phase a). In the ***boost-mode***, 3/3-PWM-ZCM is applied in the VSR-stage while the DC/DC-stage is clamped ($T_{DC,hp}$ and $T_{DC,hn}$ are permanently on to avoid switching losses and $V_{DC,p} = V_{out,p}$). In the ***transition-mode***, loss-optimal operation is still guaranteed, i.e., only three HBs are switching at any given time. In all three modes, GCC ensures essentially zero LF CM ground current ($i_{GND} \approx 0\,\text{A}$). Note that even though asymmetries are observed in two output capacitor voltages, e.g., $V_{out,p} \neq V_{out}/2$, the total output voltage V_{out} is constant.

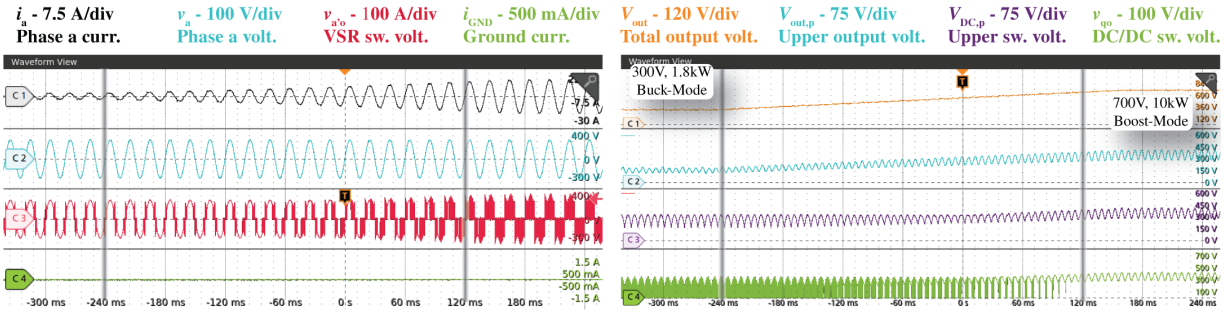

Fig. 8: Experimental waveforms of the converter shown in **Fig. 1** operating with a constant resistive load of $49\,\Omega$ and a linearly increasing output voltage $V_{out} = 300\,\text{V} \sim 700\,\text{V}$. The proposed control structure from **Fig. 5** ensures an automatic and seamless transition from the buck-mode via the transition-mode to the boost-mode. Note the different shapes of the DC-link voltage V_{DC} corresponding to the different modulation schemes, i.e., in 3/3-PWM-ZCM, $V_{DC,p} = V_{out,p}$ whereas in 1/3-PWM-ZCM, $V_{DC,p} = v_{max} = \max(v_{a'o}, v_{b'o}, v_{v'o})$.

typically dominated by the battery pack and are thus relatively large (up to several µF [12]), to the EV chassis. This could possibly lead to disturbances of other electronic components since the EV chassis as the common electric ground becomes noisy [9], [11], but can be addressed by engineering techniques, e.g., single-point ground referencing. Furthermore, these parasitic currents can be decreased by increasing the output capacitance C_{out}, e.g., considering the operating point at 400 V and 10 kW and assuming $C_{b,DC+} = C_{b,DC-} = 5\,\mu\text{F}$, the parasitic current is 210 mA rms if $C_{out} = 65\,\mu\text{F}$ but reduces to 95 mA rms if $C_{out} = 300\,\mu\text{F}$ would be used.

However, as the chassis is not only connected to the DC-link midpoint m but also to PE (see **Fig. 1**), a certain share of the leakage currents through $C_{b,DC+}$ and $C_{b,DC-}$ could also contribute to the ground current i_{GND}. Thus, the GCC monitors i_{GND} at the three-phase mains terminals and uses the VSR-stage to inject CM voltages, resulting in compensating currents to regulate i_{GND} to essentially zero. This strategy can reliably prevent nuisance trips of the RCD.

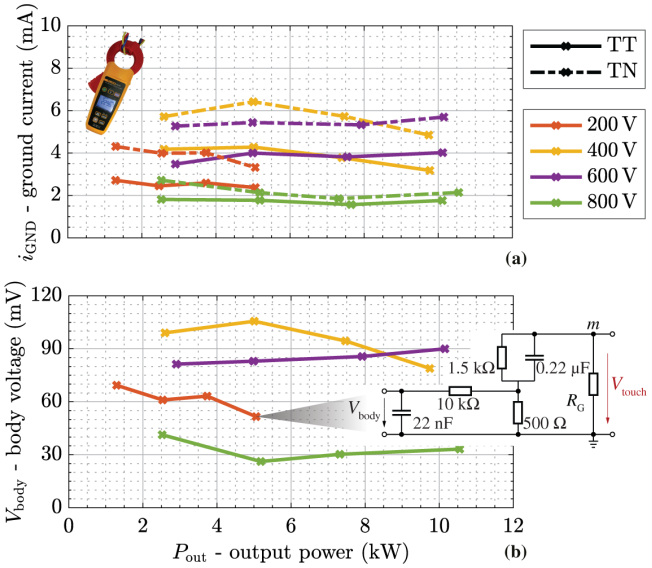

Fig. 9: (a) Ground current i_{GND} measured with a leakage current clamp meter *Fluke 368 FC* [48] and **(b)** body voltage V_{body} for operation with different output voltages from 200 V to 800 V and various power levels from 25 % to 100 % of rated load, which covers the buck-, transition-, and boost-mode. For both grid grounding schemes (TT and TN), the measured ground current remains far below typical RCD trip levels of 30 mA. In **(b)**, the body voltage V_{body} obtained by processing the measured touch voltage V_{touch} (see also **Fig. 1**) with the transfer function of the human body impedance network according to UL 2202 [49]. The highest measured body voltages of around 120 mV are well below the safe level of 250 mV defined in UL 2202 [49].

B. Ground Current and Touch Current Measurement

Fig. 9a shows the measured ground current i_{GND} at different output voltage and power levels for different operating modes. Considering that i_{GND} features an amplitude in the range of several milliamperes only, a special leakage current clamp meter *Fluke 368 FC*, specifically designed for RCD testing, is used to accurately measure i_{GND}[5]. Note that i_{GND} occurring when connected to a TN system ($R_G = R_N = 0\,\Omega$ in **Fig. 1**) is always larger than i_{GND} resulting for a connection to a TT system ($R_G = 100\,\Omega, R_N = 10\,\Omega$) due to the latter's higher grounding impedance. However, all measured values are far below the typical RCD trip levels of 30 mA [49], [50].

The standards (UL 2202, IEC 61851) also require a so-called touch current test, where an impedance network modeling the frequency-dependent impedance of the human body is connected between the local EV PE (e.g., the chassis, at the same potential as the DC output midpoint m) and true earth, i.e., across the grounding impedance R_G in **Fig. 1**, to evaluate potential electric shocks to humans [11]. The TN system's dedicated PE conductor ($R_G \approx 0$) prevents any significant voltage between the chassis and true ground (i.e., $V_{touch} \approx 0$) even for non-zero ground current so that the TN system is not considered regarding the touch current tests. Differently, in the TT system, the ground current flowing through R_G creates a potential difference that could be hazardous regarding end-user safety. **Fig. 9b** presents the body voltage V_{body} obtained by post-processing the voltage V_{touch} with the body model impedance networks' transfer function; V_{touch} is measured across the explicit resistor R_G used to realize a TT grounding system (see **Fig. 1**) for various operating points. The highest resulting $V_{body} \leq 120\,\text{mV}$ is well below the most stringent limit of 250 mV defined by UL 2202 [49].

[5]The leakage current clamp meter performs a true-rms measurement with 0.01 mA resolution, considering a frequency range of 40 Hz to 1 kHz [48].

C. Efficiency Measurement

The efficiency of the 10 kW non-isolated EV charger demonstrator is measured (Yokogawa WT3000) over the complete wide output voltage (from 200 to 800 V) and output power (from full load down to 25 % load) ranges. **Fig. 10a** shows the measured efficiency results in dependence of the output voltage and the load, where in addition, the operating points at which the efficiency measurements have been taken are indicated (linear interpolation is used in-between). **Fig. 10b** shows efficiency versus output voltage at rated power or rated output current (for low output voltages below 400 V). The measured efficiencies at most operating points are above 97 %, and at rated power (or current) are above (or around) 98 %. Furthermore, **Fig. 10b** includes estimated efficiencies of an isolated EV charger. These estimates assume an additional high-efficiency (99 % at every output voltage when delivering rated power) galvanic isolation stage cascaded with the existing high-performance PFC rectifier built in [44]. Despite this, the realized non-isolated EV charger demonstrator still exhibits relatively high operating efficiencies.

Note that the demonstrator employed here is a modified version of the system presented in [44], which features a 3-L DC/DC-stage that is not compatible with grounding the output midpoint and GCC. Compared to the 1/3-PWM-CONV, the proposed 1/3-PWM-ZCM allows zero CM injection and thus facilitates non-isolated EV charger applications, importantly, without significant increase of current or voltage stress on the semiconductors. Furthermore, as the total DC-link voltage is the same in both cases when supplying a certain output voltage, the switching losses increase caused by the voltage asymmetry, i.e., an LF 150 Hz voltage variation, between upper $V_{DC,p}$ and lower $V_{DC,n}$ DC-link voltage is limited [17]. However, compared to [44], a modification is necessary at the DC/DC-stage to enable an independent voltage regulation of the upper and lower DC-link voltages: The direct connection of the DC-link midpoint and the output midpoint results in two stacked 2-L instead of an integrated 3-L buck converter, and this requires two larger (96 µH instead of 34 µH) DM inductors. Hence, whereas perfectly suitable for experimentally verifying 1/3-PWM-ZCM, synergetic GCC, and resulting residual LF CM ground current levels, the employed demonstrator is not fully optimized regarding efficiency. Improved efficiency could be achieved with a new hardware design that takes into account non-isolated operation and, in particular, 1/3-PWM-ZCM and 3/3-PWM-ZCM.

V. Conclusion

Targeting non-isolated EV charging applications, this paper analyzes a synergetically-controlled three-phase (3-Φ) Boost-buck (Bb) voltage DC-link PFC rectifier that consists of a 3-Φ three-level (3-L) T-type (Vienna) VSR-stage cascaded by two vertically-stacked 2-L buck-type DC/DC-stages. To

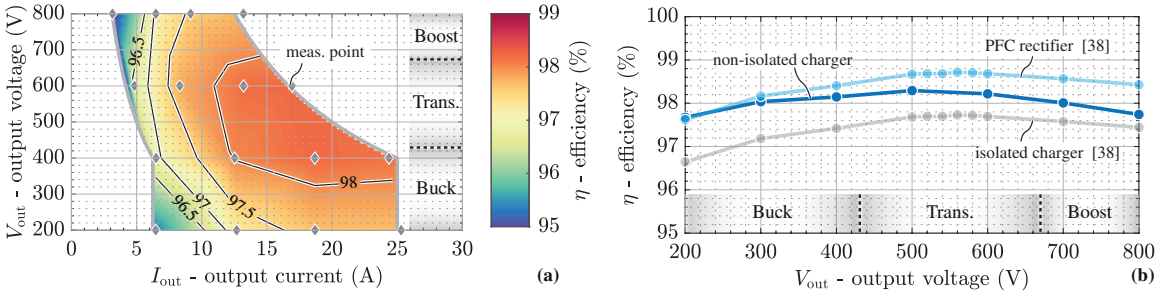

Fig. 10: Measured (Yokogawa WT3000) efficiencies of the realized 10 kW non-isolated EV charger using the proposed zero-CM loss-optimal modulation schemes (1/3-PWM-ZCM in the buck-mode and 3/3-PWM-ZCM in the boost-mode), i.e., **(a)** efficiencies with different output voltages from 200 V to 800 V and various power levels from 25 % to 100 % of rated load and **(b)** efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V). Note that estimated efficiencies of an isolated EV charger are also provided in **(b)**, assuming an additional high-efficiency (99 % at every output voltage when delivering rated power) galvanic isolation stage is cascaded with the existing PFC rectifier in [44]. Also, note that improved efficiency could be achieved with a new hardware design specifically for non-isolated operation rather than modifying existing hardware.

mitigate LF CM ground leakage currents, the wide output voltage range of 200 V to 800 V is covered by two zero CM (ZCM) PWM modulation schemes, i.e., 3/3-PWM-ZCM for boost-mode operation and the newly proposed 1/3-PMW-ZCM for buck-mode operation. Combining the two ZCM PWM schemes further achieves loss-optimal operation for any output voltage with always only three (out of five) half-bridges (HBs) actively switching (i.e., operating with PWM) and using the minimum possible DC-link voltage, i.e., resulting in the minimum possible switching losses. Furthermore, a closed-loop ground current control (GCC) is proposed to effectively suppress the LF CM current (i.e., measured as the sum of the three mains phase currents) to near zero and thus to reliably prevent the nuisance tripping of mandatory RCDs. The proposed loss-optimal operation with GCC is then experimentally verified using a 10 kW hardware demonstrator considering TT and TN mains grounding systems. All measured ground currents are below 7 mA rms and thus far below the typical RCD trip levels of 30 mA. Similarly, considering the touch current test defined in UL 2202 and the corresponding human-body impedance network, the resulting body voltages are below 120 mV, i.e., far below the standard's most stringent limit of 250 mV. Even though this hardware demonstrator is modified from an existing setup and hence not a design optimized considering operation as a non-isolated EV charger, the measured efficiencies at rated power (or rated output current for lower output voltages) are around 98% with a peak of 98.2%.

Appendix A - Controller Design

The individual controllers of the proposed synergetic control concept from **Fig. 5** are designed from the innermost controller of the DC/DC-stage buck-inductor current $I_{DC,p}$ and $I_{DC,n}$ towards the outermost controller of the output voltage V_{out} with a reduced corner frequency. The inner loop is always designed to be at least three times faster than the immediate outer one. Note that for the DC/DC-stage buck-inductor current regulator, a single P controller is implemented to avoid a runaway if clamping the DC/DC-stage (a PI controller with an anti-windup functionality is also feasible [44]).

The main synergetic cascaded controllers (including output voltage, mains current, and DC-link voltage controllers) only affect the DM behavior of the converter at the mains interface, but do not have controllability on the ground current (CM quantity). Thus, the controller corner frequencies between the synergetic DM cascaded controllers and the ground current controller are decoupled. Furthermore, the system modeling and the PI controller tuning for the GCC are conducted based on [35] and are not detailed here for the sake of brevity. **Tab. II** shows the final implemented controller parameters in the form of

$$G(s) = k_p \cdot (1 + 2\pi f_c \cdot \frac{1}{s}).$$

TABLE II: Implemented controller parameters of the realized non-isolated 3-Φ Bb voltage DC-link EV charger.

Output voltage	k_p	gain	1.8
	f_c	corner frequency	6
Input current	k_p	gain	2.85
	f_c	corner frequency	25
DC-link voltage	k_p	gain	0.18
	f_c	corner frequency	75
Buck inductor current	k_p	gain	2.5
Ground current	k_p	gain	9.65
	f_c	corner frequency	325

Appendix B - Operation Under Irregular Mains Conditions

This Appendix analyzes and verifies the resilient operation of the proposed GCC for the non-isolated 3-Φ Bb voltage DC-link EV charger (see **Fig. 1**) under two representative irregular mains conditions considering the TN grounding system (the worst case for ground currents), e.g., asymmetric mains voltage amplitudes (±10%) [50] and mains voltages with low-frequency harmonic distortions [51]. Loss-optimal operation enabled by the proposed 1/3-PWM-ZCM is still maintained, i.e., both the VSR-stage and the DC/DC-stage operate with the minimum possible DC-link voltage and with the minimum number (three out of five) of HF-switching HBs. Even though a slight increase is observed compared to ideal mains conditions, the simulated ground current within the considered frequency range of 40 Hz to 1 kHz remains far below typical RCD trip levels of 30 mA for both cases.

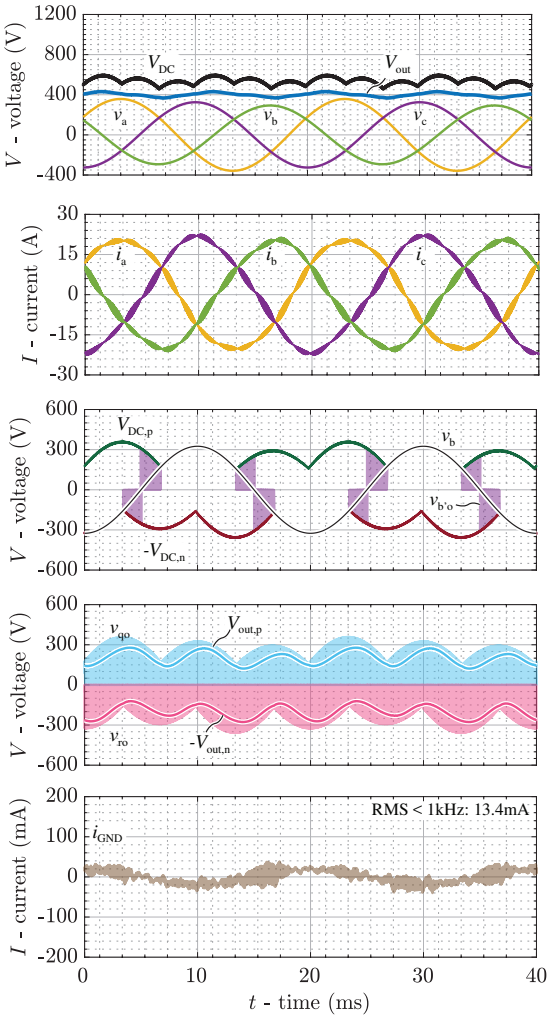

Fig. 11: Simulated key waveforms of the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1** operating in buck-mode with 1/3-PWM-ZCM (buck-mode) under asymmetric 3-Φ mains voltage amplitudes, i.e., $+10\%$ in phase a and -10% in phase c [50], to supply a 400 V, 10 kW load. The phase-b switched voltage of the VSR-stage, $v_{b'o}$, confirms 1/3-PWM of the VSR-stage, whereas the switched output voltages, v_{qo} and v_{ro}, indicate the HF-switching of both DC/DC-stage HBs. The simulated ground current within the considered frequency range of 40 Hz to 1 kHz remains far below typical RCD trip levels of 30 mA.

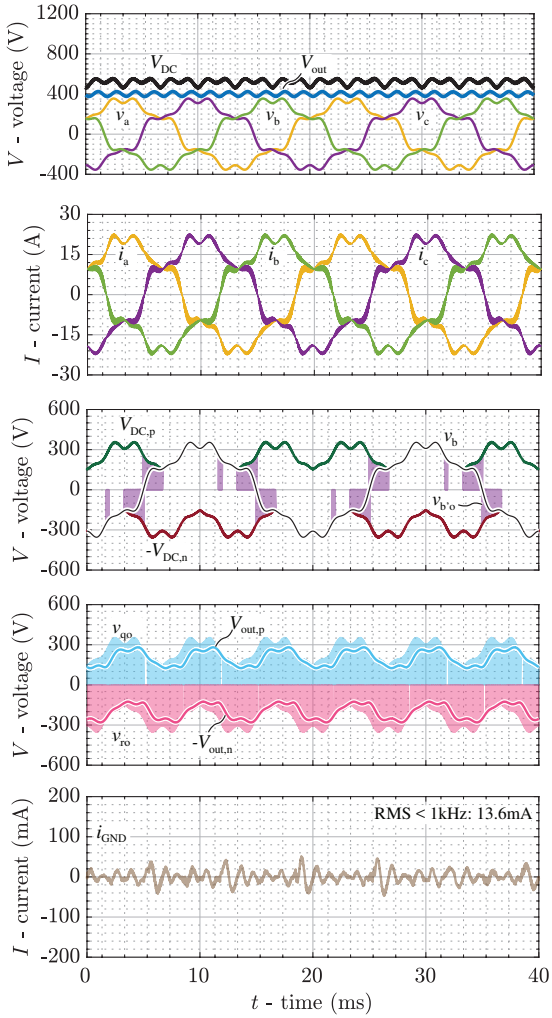

Fig. 12: Simulated key waveforms of the non-isolated 3-Φ Bb voltage DC-link EV charger shown in **Fig. 1** operating with 1/3-PWM-ZCM (buck-mode) under with distorted mains voltages, i.e., the 3-Φ mains voltages contain 12% of 5th, 10% of 7th, and 7% of 11th harmonics [51], to supply a 400 V, 10 kW load. The phase-b switched voltage of the VSR-stage, $v_{b'o}$, confirms 1/3-PWM of the VSR-stage, whereas the switched output voltages, v_{qo} and v_{ro}, indicate the HF-switching of both DC/DC-stage HBs. The simulated ground current within the considered frequency range of 40 Hz to 1 kHz remains far below typical RCD trip levels of 30 mA.

Specifically, **Fig. 11** verifies the resilient operation of the non-isolated 3-Φ Bb voltage DC-link EV charger under asymmetric 3-Φ mains voltages, i.e., voltage amplitudes $+10\%$ in phase a and -10% in phase c [50]. In the buck-mode operation with an output voltage of 400 V, the upper and lower DC-link voltages are shaped *individually* by the DC/DC-stage such that the upper (lower) DC-link voltage follow v_{max} ($-v_{min}$) to achieve the 1/3-PWM operation of the VSR-stage without any LF CM injection, and, at any given point in time, only one of the VSR-stage's three bridge-legs operates with HF PWM such that a considerable switching loss reduction is achieved. Similar results are observed in **Fig. 12**, which shows the operation of the proposed GCC when several voltage harmonics, e.g., 12% of 5th, 10% of 7th, and 7% of 11th, are added on top of the 3-Φ sinusoidal mains voltages [51].

REFERENCES

[1] J.-P. Rodrigue, *The geography of transport systems*. Routledge, 2020.
[2] *STRIA Roadmap on Transport Electrification (ELT)*, European Commission, Accessed: 2023-02-11. [Online]. Available: https://shorturl.at/knwE1
[3] Y. Wu, Z. Wang, Y. Huangfu, A. Ravey, D. Chrenko, and F. Gao, "Hierarchical operation of electric vehicle charging station in smart grid integration applications—An overview," *Int. J. Electr. Power Energy Syst.*, vol. 139, p. 108005, 2022.
[4] C. Stutz, S. Nielebock, and M. März, "Analytic calculation of touch and leakage currents of non-isolated EV chargers using a fast common mode calculation method and non-ideal passive component models," in *Proc. IEEE 24th Europ. Conf. Power Electron. Appl. (EPE/ECCE Europe)*, Hanover, Germany, Sep. 2022.
[5] A. Albanna, M. N. Arafat, A. Gupta, M. Anwar, and M. Teimor, "Analysis of ground fault currents in isolated and non-isolated charging modules in electric vehicles," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Dearborn, MI, USA, Jun. 2015.
[6] N. Sakr, D. Sadarnac, and A. Gascher, "A review of on-board integrated chargers for electric vehicles," in *Proc. Europ. Conf. Power Electron. Appl. (EPE/ECCE Europe)*, Lappeenranta, Finland, Aug. 2014.
[7] S. Loudot, B. Briane, O. Ploix, and A. Villeneuve, "Fast charging device for an electric vehicle," U.S. Patent 8 847 555B2, Sep. 30, 2014.

[8] L. Zhou and M. Preindl, "Bidirectional transformerless EV charging system with low device cost and leakage current," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Portland, OR, USA, Sep. 2018.

[9] Y. Zhang, G. Yang, X. He, M. Elshaer, W. Perdikakis, H. Li, C. Yao, J. Wang, K. Zou, Z. Xu, and C. Chen, "Leakage current issue of non-isolated integrated chargers for electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Portland, OR, USA, Sep. 2018.

[10] C. Viana, S. Semsar, M. Pathmanathan, and P. W. Lehn, "Generalized method for designing nonisolated safety standard compliant onboard chargers for electric vehicles," in *Proc. 47th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Toronto, Canada, Oct. 2021.

[11] J. Wang, Y. Zhang, M. Elshaer, W. Perdikakis, C. Yao, K. Zou, Z. Xu, and C. Chen, "Nonisolated electric vehicle chargers: Their current status and future challenges," *IEEE Electrific. Mag.*, vol. 9, no. 2, pp. 23–33, 2021.

[12] B. Strothmann, F. Schafmeister, and J. Bocker, "Common-mode-free bidirectional three-phase PFC-rectifier for non-isolated EV charger," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Phoenix, AZ, USA, Jun. 2021.

[13] M. Jahnes, L. Zhou, M. Eull, W. Wang, and M. Preindl, "Design of a 22 kW transformerless EV charger with V2G capabilities and peak 99.5% efficiency," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, Jun. 2022.

[14] M. Eull, L. Zhou, M. Jahnes, and M. Preindl, "Bidirectional nonisolated fast charger integrated in the electric vehicle traction drivetrain," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 1, pp. 180–195, Mar. 2022.

[15] C. Viana, S. Semsar, M. Pathmanathan, and P. W. Lehn, "Integrated transformerless EV charger with symmetrical modulation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12 506–12 516, Dec. 2022.

[16] L. Zhou, M. Jahnes, M. Eull, W. Wang, and M. Preindl, "Control design of a 99% efficiency transformerless EV charger providing standardized grid services," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4022–4038, Apr. 2022.

[17] D. Zhang, D. Cao, J. Huber, J. Everts, and J. W. Kolar, "Non-isolated three-phase current DC-link buck-boost EV charger with virtual output midpoint grounding and ground current control," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 1398–1413, Mar. 2024.

[18] C. Shi and A. Khaligh, "A two-stage three-phase integrated charger for electric vehicles with dual cascaded control strategy," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 898–909, Jan. 2018.

[19] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[20] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1016–1026, Feb. 2016.

[21] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," *"IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3306–3324, 2019.

[22] Y. Park, S. Chakraborty, and A. Khaligh, "DAB converter for EV onboard chargers using bare-die SiC MOSFETs and leakage-integrated planar transformer," *IEEE Trans. Transp. Electrification.*, vol. 8, no. 1, pp. 209–224, 2021.

[23] R. Pradhan, N. Keshmiri, and A. Emadi, "On-board chargers for high-voltage electric vehicle powertrains: Future trends and challenges," *IEEE Open J. Power Electron.*, 2023.

[24] J. Yuan, A. Poorfakhraei, Y. Zhang, G. Fang, C. Liu, and A. Emadi, "An improved adaptive sinusoidal single phase shift modulation for bidirectional single-stage onboard EV chargers," *IEEE Trans. Transp. Electrification.*, 2023.

[25] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51 501–51 518, 2021.

[26] N. Hou, J. Hu, D. Mou, Y. Zhang, Y. W. Li, and R. W. De Doncker, "A simple DC-offset eliminating method of the series-inductance current for the DAB DC-DC converter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4224–4228, 2022.

[27] Z. Ye, C. Li, J. Liu, and Z. Zheng, "Towards full range zero-voltage switching of DAB converters: An improved multi-mode modulation at light loads under close-to-unity voltage ratio," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 6912–6917, 2023.

[28] J. Hu, S. Cui, S. Wang, and R. W. De Doncker, "Instantaneous flux and current control for a three-phase dual-active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 2184–2195, 2019.

[29] Y. Li, J. A. Anderson, M. Haider, J. Schäfer, J. Miniböck, J. Huber, G. Deboy, and J. W. Kolar, "Optimal synergetic operation and experimental evaluation of an ultra-compact gan-based three-phase 10 kW EV charger," *IEEE Trans. Transp. Electrification.*, 2023, early access.

[30] D. Lyu, C. Straathof, T. B. Soeiro, Z. Qin, and P. Bauer, "ZVS-optimized constant and variable switching frequency modulation schemes for dual active bridge converters," *IEEE Open J. Power Electron.*, vol. 4, pp. 2644–1314, Sep. 2023.

[31] Y. Bi, T. Zhao, J. Xu, G. Shu, C. Wu, Y. Wang, and T. B. Soeiro, "An improved combined current control for single-phase operation mode of single-/three-phase EV charging system with voltage ripple suppression," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13 635–13 649, Nov. 2023.

[32] A. Zade, C. R. Teeneti, M. Mansour, S. Gurudiwan, B. Hesterman, H. Wang, and R. Zane, "A 21-kW unfolding-based single-stage AC-DC converter for wireless charging applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 1, pp. 8–27, Jan. 2024.

[33] H. Zhu, S. Hu, M. Tahir, Y. Bai, and X. Wu, "CLLC modeling and control in V2G mode to mitigate double line frequency current for high power density on-board charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 1, pp. 219–230, Feb. 2023.

[34] V. P. Maurya, A. K. Pratihasta, and R. K. Singh, "A multimode on-board charger with multiport outputs and reduced switch count for EVs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 263–273, Jan. 2023.

[35] D. Boillat, F. Krismer, and J. W. Kolar, "Ground current control scheme for back-to-back three-phase T-type rectifier and inverter systems," *IEEJ Trans. Ind. Appl.*, vol. 138, no. 11, pp. 1–5, 2018.

[36] R. Joensson, "A new switch circuit for frequency inverters," in *Proc. Int. Conf. Power Electron. Intelligent Motion (PCIM)*, Tokyo, Japan, Dec. 1988.

[37] J. W. Kolar and H. Ertl, "Voltage converter device for a D.C. voltage consumer and a method for supplying the consumer," GB Patent 2 258 958B, Jan., 1996.

[38] D. Rendusara and P. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1135–1143, Nov. 1998.

[39] D. Zhang, M. Guacci, J. W. Kolar, and J. Everts, "Three-phase bidirectional ultra-wide output voltage range current DC-link AC/DC buck-boost converter," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Singapore, Oct. 2020, pp. 4709–4716.

[40] A. L. Julian, G. Oriti, and T. A. Lipo, "Elimination of common-mode voltage in three-phase sinusoidal power converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 982–989, Sep. 1999.

[41] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Investigation of fourth-leg for common-mode noise reduction in three-level neutral point clamped inverter fed motor drive," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Anaheim, CA, USA, Mar. 2019.

[42] D. Zhang, J. Huber, and J. W. Kolar, "A three-phase synergetically controlled buck-boost current DC-link EV charger," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15 184–15 198, Dec. 2023.

[43] J. Azurza A., M. Haider, D. Bortis, J. W. Kolar, M. Kasper, and G. Deboy, "New synergetic control of a 20 kW isolated Vienna rectifier front-end EV battery charger," in *Proc. 20th IEEE Workshop Control Modeling Power Electron. (COMPEL)*, Toronto, Canada, Jun. 2019.

[44] D. Zhang, C. Leontaris, J. Huber, and J. W. Kolar, "Optimal synergetic control of three-phase/level boost-buck voltage DC-Link AC/DC converter for very-wide output voltage range high-efficiency EV charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, 2023, early access.

[45] K. Rigbers, S. Schroder, R. De Doncker, P. Lurkens, M. Wendt, and U. Boke, "High-efficient soft-switching converter for three-phase grid connections of renewable energy systems," in *Proc. Int. Conf. Power Electon. Drive Syst. (PEDS)*, Kuala Lumpur, Malaysia, Nov. 2005, pp. 246–250.

[46] P. Luerkens, M. Wendt, T. Duerbaum, and H. van der Broeck, "3-phase solar converter circuit and method," U.S. Patent 7 539 029, May, 2009.

[47] Q. Lei and F. Z. Peng, "Space vector pulse width amplitude modulation for a buck–boost voltage/current source inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 266–274, Jan. 2014.

[48] *368/368 FC and 369/369 FC leakage current clamp meters*, Fluke Corporation, 2016.

[49] *Standard for safety: Electric vehicle (EV) charging system equipment*, UL Std. 2202, 2012.

[50] *Electric vehicle conductive charging system - Part 1: General requirements*, IEC Std. 61 851-1, 2017.

[51] *Electromagnetic compatibility (EMC) - Part 2-4: Environment - Compatibility levels in industrial plants for low-frequency conducted disturbances*, IEC Std. 61 000-2-4, 2002.