VIENNA Rectifier II—A Novel Single-Stage High-Frequency Isolated Three-Phase PWM Rectifier System

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***Abstract*— Based on an analysis of basic realization possibilities, the structure of the power circuit of a new single-stage three-phase boost-type pulsewidth modulated (PWM) rectifier system (VIENNA Rectifier II) is developed. This system has continuous sinusoidal time behavior of the input currents and high-frequency isolation of the output voltage, which is controlled in a highly dynamic manner. As compared to a conventional two-stage realization, this system has substantially lower complexity and allows the realization of several isolated output circuits with minimum effort. The basic function of the new PWM rectifier system is described based on the conduction states occurring within a pulse period. Furthermore, a straightforward space-vector-oriented method for the system control is proposed which guarantees a symmetric magnetization of the transformer. Also, it makes possible a sinusoidal control of the mains phase currents in phase with the associated phase voltages. By digital simulation, the theoretical considerations are verified and the stresses on the power semiconductors of the new converter system are determined. Finally, results of an experimental analysis of a 2.5-kW laboratory prototype of the system are given, and the direct startup and the short-circuit protection of the converter are discussed. Also, the advantages and disadvantages of the new converter system are compiled in the form of an overview.**

***Index Terms*— High-frequency isolation, single-stage ac-to-dc power conversion, three-phase high-power-factor rectifier, VIENNA rectifier.**

I. Introduction

THREE-PHASE power supply modules for telecommunication systems are designed in a two-stage concept in most cases [1]. This means that the following partial tasks are realized by a three-phase pulsewidth modulated (PWM) rectifier input stage:

- power-factor correction (ideal sinusoidal control of the mains phase currents in phase with the associated phase voltages, i.e., resistive fundamental behavior and low total harmonic distortion (THD) and/or guaranteeing electromagnetic compatibility concerning low-frequency mains current harmonics [2], [3]);
- rectification.

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The following tasks are handled by a dc-to-dc converter output stage connected in series:

- high-frequency isolation of the output voltage;
- matching of the input and output voltage levels (rated voltage of the European low-voltage mains, 400 V_{rms} line-to-line; rated dc output voltage, 48 or 60 V) via winding ratio of the transformer;
- tight, highly dynamic control of the output voltage and/or of the power flow on the output side (avoidance of low-frequency harmonics in the output quantities and/or of psophometric noise).

The advantages of this concept are the following:

- separate optimizability of the converter stages concerning operational mode and dimensioning (e.g., applicability of already proven control methods, power supply to the output stage with constant voltage, independent of mains voltage variations, etc.);
- possibility of a separate development of the input and output stages;
- simple buffering of short mains failures due to providing a capacitor of appropriate capacity in the voltage dc link (at high voltage level).

However, the following disadvantages have to be mentioned:

- relative high complexity of the entire power and control circuit (high number of power semiconductors and filter elements, separate controls for each converter stage), meaning a relatively high realization effort;
- twofold power conversion and, therefore, possibly reduction of the efficiency of the overall system.

Due to the following requirements being characteristic for telecommunications power supplies, it, therefore, seems to be obvious to consider possibilities of omitting the filter elements in the dc link of the conventional two-stage solutions and/or of a realization of *single-stage* three-phase ac-to-dc converters with *high-frequency* isolation of the output voltage:

- high efficiency of the energy conversion (low energy costs for continuous operation and low effort for air conditioning of the power supply apparatus and/or switching centers);
- high power density (W/cm^3) and/or low specific weight (W/kg) and/or low space requirement and/or simple portability;

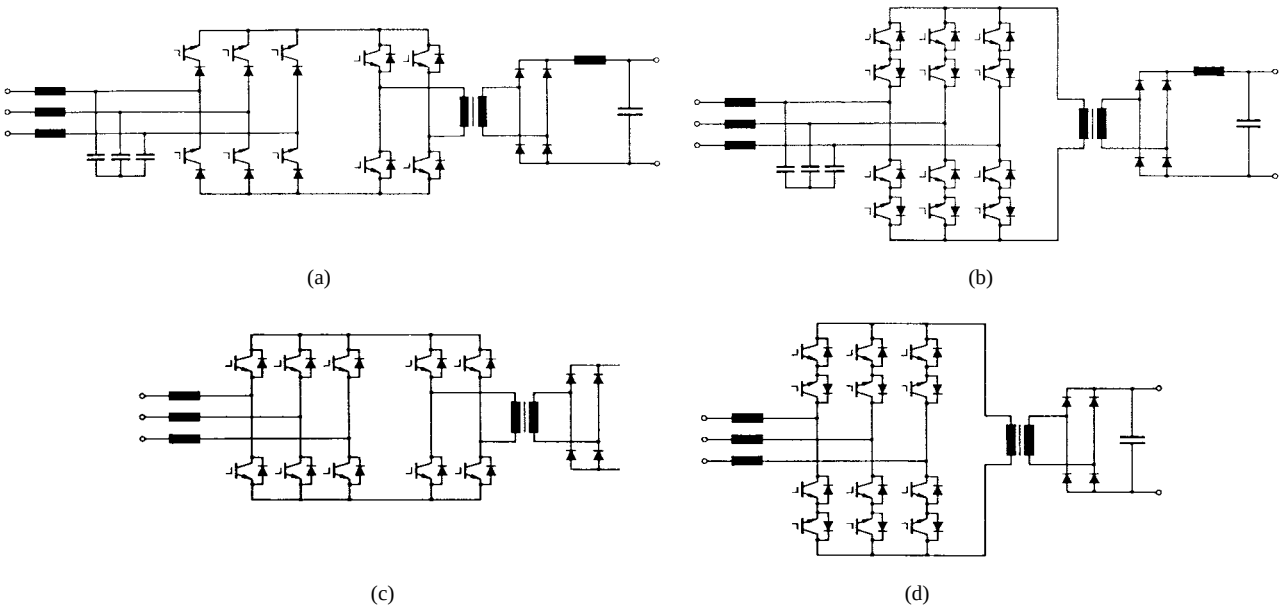


Fig. 1. Basic structures of three-phase single-stage high-frequency isolated PWM rectifier systems. (a) and (b) Quasi-single-stage buck-derived bridge and single-stage buck-derived matrix PWM rectifier system according to [11]. (c) and (d) Quasi-single-stage boost-derived bridge and single-stage boost-derived matrix PWM rectifier system according to [12] (naming of the systems according to [10]).

- high reliability;
- low production costs.

Remark: Basically, the isolation of the output circuit also could be achieved by a mains-side transformer. As shown in [4], this would make realizable a single-stage ac-to-dc converter with a sinusoidal input current shape in an elegant way. However, because, in particular, for telecommunications systems a high power density is desired, in the case at hand, only circuit concepts with high-frequency isolation are considered. Also, with regard to high power density, the further considerations are limited to direct three-phase systems. This is the case because three-phase converters built up of three two-stage [5] or single-stage [6] converters arranged in star or delta connection show a relatively low utilization of the power semiconductors and of the transformers due to the power flow of each phase pulsating with twice the mains frequency [7, Sec. II-A], [8].

Topologies of single-stage, high-frequency isolated three-phase PWM rectifier systems can be formed (as proposed in [9]) by replacing the input part of basic dc-to-dc converter structures by a three-phase six-switch boost or a six-switch buck PWM rectifier system (self-commutated three-phase bridge circuits with voltage and/or current output [10, Fig. 1]). There, with consideration of the blocking voltage stress on the valves, in particular, the combinations with dc-to-dc converter bridge circuits (as proposed and analyzed in principle in [11] and [12]) are of interest [quasi-single-stage bridge PWM rectifier systems, see Fig. 1(a) and (c)]. As further alternate circuit variants with the same basic function, we want to mention the three-phase buck-derived isolated matrix PWM rectifier system [11], as shown in Fig. 1(b), and the three-phase boost-derived isolated matrix PWM rectifier system [12], as shown in Fig. 1(d). There, the primary winding of the high-frequency transformer is fed via a three-phase-to-single-phase ac-to-ac matrix converter. This converter is built up with bidirectional and bipolar (four quadrant) turn-off power switching elements. For the systems according to Fig. 1(a) and (b) (buck derived), the current switched and being injected into the mains by the switching elements on the primary is impressed by the output inductance; for the systems according to Fig. 1(c) and (d) (boost derived), the voltage being required for controlling the mains current is impressed by the output capacitor (no output inductor has to be provided).

Remark: For small output voltages and/or high output currents (e.g., for telecommunications power supply modules of higher power), the secondary circuit is realized in most cases as a center-tapped circuit and not as a full-bridge circuit (reduction of the conduction losses), as shown in Fig. 1.

An interesting alternate realization of a three-phase-to-single-phase ac-to-ac converter with exclusive application of 12 bidirectional unipolar turn-off power semiconductors—insulated gate bipolar transistors (IGBT's) with antiparallel freewheeling diodes—has been proposed in [13]. This, however, cannot be treated here in more detail for the sake of brevity.

For the realization of a single-stage three-phase ac-to-dc converter with high-frequency isolation, one basically could use (besides the already-mentioned circuit concepts) also the Cuk-based or SEPIC-based single-switch converters as proposed in [14]–[16] or single-switch three-phase flyback convertes as proposed in [17]. These converters show a very simple structure of the power and control circuits which is paid for, however, by a high voltage and current stress on the devices [18] and by a relatively high filtering effort for suppressing electromagnetic interferences [19] (discontinuous input current shape). The systems are economically applicable, therefore, only for output power levels <5 kW and/or they are of minor importance for the realization of high-power telecom-

munications power supply modules (output power typically $6 \cdots 12$ kW, i.e., 60 V/$100 \cdots 200$ A). Therefore, they are not described in greater detail in this paper.

Details of the operation, the control, and the dimensioning of the buck-derived single-stage matrix PWM rectifier system are discussed in [20]-[22]. The buck-derived isolated quasi-single-stage bridge PWM rectifier system according to Fig. 1(a) is treated in [10] in detail. On the other hand, three-phase isolated (quasi-) single-stage *boost*-derived bridge PWM rectifier systems have not been analyzed in detail so far. This is explained in [10] by the following:

- higher blocking voltage stress on the valves;
- the problem of startup of the converter systems (lack of the voltage required for the control and/or limitation of the input current in case of output capacitor not charged);
- the problem of overload protection (current limitation for short circuit of the output voltage) or of overcurrent limitation for mains overvoltages.

However, boost-derived converter systems show a series of advantages as compared to buck-derived systems, such as the following:

- continuous shape of the input current (therefore, no input filter capacitors have to be provided);
- direct control of the mains current, i.e., of the input quantity being of special interest with regard to effects on the mains (the input current of buck-derived PWM rectifier systems is defined indirectly, i.e., via the difference between mains voltage and the controlled input filter capacitor voltage);
- no danger of a direct short circuit of a mains line-to-line voltage;
- impressed transformer primary current, therefore, contrary to buck-derived converter structures, no danger of high overcurrent spikes due to magnetic core saturation or high reverse-recovery time of the diodes on the output side;
- direct voltage output (no output inductor required and/or simple realizability of several isolated output circuits); the output voltage directly defines the blocking voltage across the diodes on the secondary (the blocking voltage is independent of the input voltage).

These advantages ultimately form the basis for the wide applicability of this circuit type in connection with *single-phase* single-stage [23]–[25] and two-stage power-factor correction [26].

Based on this contradiction, a closer and objective analysis and assessment of the practical applicability of three-phase boost-derived single-stage isolated PWM rectifier systems seems of special interest.

In this paper, based on a step-by-step simplification of the circuit proposed in [12] [see Fig. 1(c)], a new topology of a three-phase single-stage high-frequency isolated PWM rectifier system [VIENNA Rectifier II, see Figs. 2(d) and 3] with minimum complexity of the power circuit is derived (see Section II). In Section III, the basic function of the PWM rectifier system is described based on the conduction states occurring within a pulse period. Furthermore, a straightforward space-vector-oriented method for the system control is proposed which guarantees a symmetric magnetization of the transformer. Also, it makes possible a sinusoidal control of the mains phase currents in phase with the associated phase voltages (see Section IV). There, the amplitude of the phase currents is given by the output voltage control system. By digital simulation (see Section V), the theoretical considerations are verified and, in Section VI, results of an experimental analysis of a 2.5-kW laboratory prototype of the system are given and possibilities of a low-loss limitation of switching overvoltages occurring due to nonideal coupling of the primary and secondary windings of the transformer are discussed, as well as the direct startup and the short-circuit protection of the converter. Also, the advantages and disadvantages of the new converter system are compiled in the form of an overview (see Section VII).

II. Derivation of the Circuit Topology

A three-phase boost-type ac-to-dc converter system with sinusoidal current input and high-frequency isolation of the output voltage is realized, as already mentioned in Section I in the conventional way as a two-stage voltage dc-link converter, i.e., by coupling on the dc side of a PWM rectifier system and of a dc-to-dc converter system [see Fig. 2(a)].

As proposed in [12], the structure of this relatively complex system can be simplified by omitting the dc-link capacitor C and/or by replacing the two-stage converter by a quasi-single-stage topology [see Fig. 2(b)]. Then, the dc-to-dc converter stage is operated with impressed current and not with impressed voltage. Therefore, at the output of the dc-to-dc converter, no inductor L_O is required to handle the difference between transformed dc-link voltage and output voltage [see Fig. 2(b)]. (It is important to note that the dc-link capacitor serves only for smoothing power oscillations with switching frequency for symmetric three-phase systems and sinusoidal shape of the input quantities, i.e., the resulting quasi-single-stage converter system has (ideally) a time-constant power flow for averaging over processes with switching frequency despite lacking a dc-link capacitor.) However, this circuit modification does not reduce the number of turn-off power semiconductors. Therefore, the system realization is still connected with a relatively high effort, and possibilities of a further reduction of the circuit complexity have to be searched for.

A starting point for this is given by the fact that the PWM rectifier stage basically would allow a reversal of the power flow (energy feedback from the dc link into the mains); the system operation is limited to rectifier operation, however, due to the unidirectionality of the dc-to-dc converter output stage. Therefore, the bidirectional input stage can be replaced by a unidirectional PWM rectifier system as proposed in [27] (see [27, Fig. 2]); this allows us to halve the number of turn-off power semiconductors of the rectifier stage [see Fig. 2(c)]. Furthermore, this leads to a higher utilization of the power semiconductors because each power transistor of a phase participates in conducting current during the positive *and* negative and not only during one current half wave.

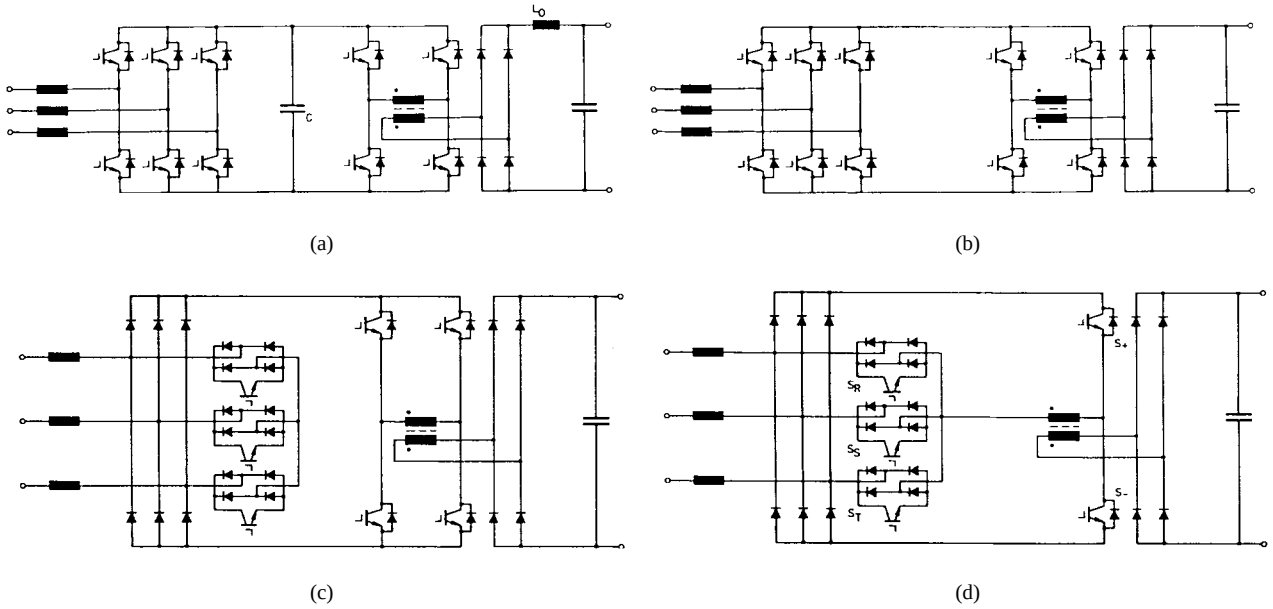


Fig. 2. Derivation of the basic structure of a new single-stage boost-type high-frequency isolated PWM rectifier system [see (d)] based on a conventional two-stage converter system with voltage dc link [see (a)].

Due to the structure of the circuit received thereby, it is obvious to transfer partially the function of the dc-to-dc converter output stage to the input stage in a further step, i.e., the switchover of a terminal of the primary winding of the transformer between positive and negative dc-link bus will be performed by the input stage. The now resulting novel topology of a *single-stage* (because sections of the mains phase currents are fed directly via the primary winding and the energy is transferred directly to the secondary) boost-derived three-phase ac-to-dc converter with high-frequency isolation is shown in Fig. 2(d). With the exception of a ripple with switching frequency, this system allows a sinusoidal mains current control in phase with the mains voltage; accordingly, an (ideally) constant output power results.

One has to note, however, that the reduction of the complexity of the power circuit as compared to the circuit according to Fig. 2(b) and the transition to direct and/or single-stage energy transfer results in higher complexity of the system control because now the switches S_R, S_S, S_T, and S_+ and S_- have to guarantee (in immediate interaction) a sinusoidal mains current shape and a pure alternating magnetization with switching frequency for the transformer magnetic core.

For the derivation of a control law for the circuit shown in Fig. 2(d), in the following, the space vectors $\boldsymbol{U}_{U,j}$ of the rectifier input voltage, resulting for the different switching states j, and the variation of the transformer magnetization are analyzed. There, a modified realization of the proposed circuit is taken as reference (see Fig. 3) which is being obtained by the integration of the four-quadrant switches into the bridge legs of the input diode bridge [28]. The topology of the input stage is then identical to a three-level PWM rectifier system which has been proposed in [29] (see [29, Fig. 9]) and which has been introduced in the literature as the VIENNA Rectifier. Accordingly, the circuit proposed here will be called the *VIENNA Rectifier II*. However, it has two-level (and not three-level) characteristic concerning voltage generation at the input, contrary to the system described in [29]. The advantage of the realization variant shown in Fig. 3 [as compared to the circuit of Fig. 2(d)] is that it allows a limitation of the blocking voltages of all valves by a simple overvoltage limitation circuit situated between positive and negative dc-link bus (see Section VI-C). Furthermore, one can then obtain a freewheeling of the transformer magnetizing current (and of the mains phase currents) by switching on the switches S_+ and S_-, i.e., one is not constrained by the switching state of the switching elements $S_i, i = R, S, T$ (see Section IV-B), simplifying the system control.

III. Basic Principle of Operation

Because a mains phase current $i_{N,i} > 0, i = R, S, T$, flows through the associated freewheeling diode $D_{F+,i}$ for turned-off power transistor S_i and through $D_{F-,i}$ for $i_{N,i} < 0$, the voltage generation at the input side of the system is determined not only by the switching states of the power transistors but also by the signs and (as shown in the following) also by the ratios of the phase current magnitudes. The same is true for the polarity of the voltage across the power transformer being defined by the sign of the primary current $i_{T,1}$ (which is formed from sections of the phase currents). However, due to the symmetries of the circuit and of the feeding three-phase voltage system $u_{N,i}$ for analyzing of a sign combination of the phase currents (e.g., $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$ being valid within a $\pi/3$-wide interval of the mains period) the relationships within the entire mains period are covered.

A. Assumptions

In the following, the stationary relations for $i_{N,R} > 0$, $i_{N,S} < 0$, and $i_{N,T} < 0$ and/or for an angle interval $\varphi_N = (-(\pi/6), +(\pi/6))$ are considered. There, the considerations

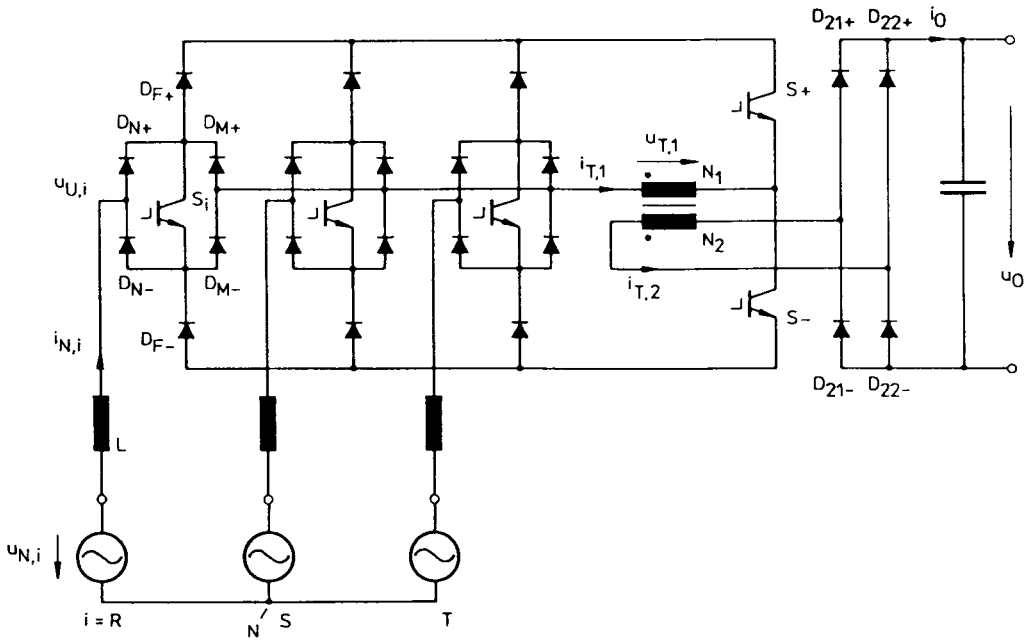


Fig. 3. The considerations of this paper are based on the shown realization variant of the proposed three-phase single-stage high-frequency isolated boost-type PWM rectifier system. The circuit is obtained by the integration of the four-quadrant switches of the circuit according to Fig. 2(d) into the bridge legs of the input diode bridge. The basic system function is not influenced by this modification. The feeding three-phase mains is shown in the form of voltage sources $u_{N,i}, i = R, S, T$.

are based on purely sinusoidal mains current shapes

$$\begin{aligned} i_{N,R} &= \hat{I}_N \cos(\varphi_N) \\ i_{N,S} &= \hat{I}_N \cos\left(\varphi_N - \frac{2\pi}{3}\right) \\ i_{N,T} &= \hat{I}_N \cos\left(\varphi_N + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

where

$$\varphi_N = \omega_N t \tag{2}$$

($\omega_N = 2\pi f_N$ denotes the mains angular frequency) in order to limit the derivations to the essentials. This means that the mains current ripple is neglected, and only the fundamental is considered. Furthermore, resistive mains fundamental behavior is assumed, i.e., currents $i_{N,i}, i = R, S, T$, and mains phase voltages $u_{N,i}$ (having also a purely sinusoidal shape) are in phase. Then, we have for the space vector of the mains current and voltage

$$\begin{aligned} \underline{i}_N &= \hat{I}_N \exp j\varphi_N \\ \underline{u}_N &= \hat{U}_N \exp j\varphi_N. \end{aligned} \tag{3}$$

Remark: The space vector related to a triple of phase quantities is calculated according to the defining equation (shown for the example of the mains voltage)

$$\underline{u}_N = \frac{2}{3}(u_{N,R} + \underline{a}u_{N,S} + \underline{a}^2 u_{N,T}), \qquad \underline{a} = \exp j\frac{2\pi}{3}. \tag{4}$$

The transformer is assumed ideal, i.e., stray inductance L_σ, magnetizing current i_m (with the exception of Sections IV-A and IV-B we assume for the magnetizing inductance $L_m \to \infty$ and/or $i_m \to 0$), winding resistances, and winding capacitances are neglected. This means that the real transformer is replaced by an ideal transformer with a transformation ratio being equal to the turns ratio N_1/N_2 (see Fig. 4). Furthermore, parasitic capacitances of the valves are neglected and/or, in general, idealized valves are assumed (no forward voltage drop, negligible switching times, in particular, no reverse-recovery current for diodes, etc.). Then, the analysis of oscillations following switching processes between L_σ and parasitic capacitances and the inclusion of an overvoltage limitation circuit (see Section VI-C) can be excluded from the considerations. Furthermore, the output voltage u_O is assumed to be impressed and constant $u_O = U_O$.

B. System Switching States and Voltage Generation

For the denomination of the switching state of the power transistors S_R, S_S, S_T, and S_+, S_-, switching functions s_R, s_S, s_T, and s_+, s_- are used in the following. There, $s_i = 1$ corresponds to the on state and $s_i = 0$ to the off state. A characterization of the switching state of the overall system can then be made in a clear form by using the combinations $j = (s_R s_S s_T)_{s_+ s_-}^{\mathrm{sign}\{u_{T,1}\}}$. It represents, besides the switching state of the transistors, also a characterization concerning the direction of the current flow $i_{T,1}$ in the primary N_1 of the transformer and/or the sign of the voltage $u_{T,1}$ across N_1 (given by $\mathrm{sign}\{u_{T,1}\} = +$ or $-$; for $u_{T,1} = 0, \mathrm{sign}\{u_{T,1}\} = 0$ is defined).

As becomes immediately clear, the control of the power transistors S_+ und S_- has to be performed dependent on the sign of the phase currents $i_{N,i}$, e.g., for turning off a switch S_i conducting positive current $i_{N,i} > 0$, one has to turn on S_+ in any case and S_- for turning off a switch S_i conducting negative current $i_{N,i} < 0$ (s_+ or $s_- \to 1$) in

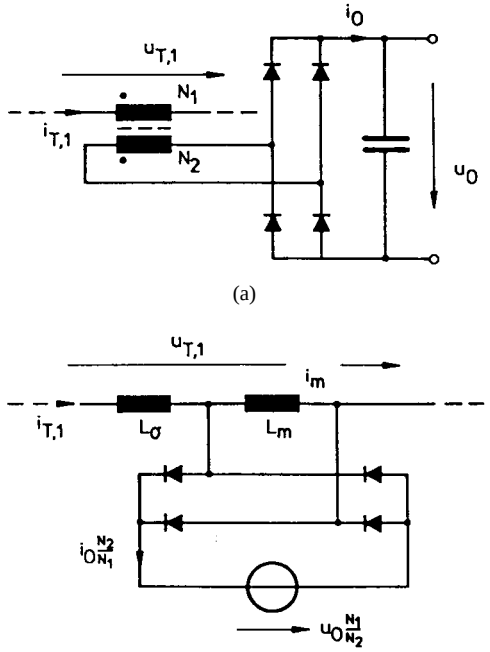


Fig. 4. Idealizations of the transformer and the output circuit of the system assumed for the basic considerations of this paper. (a) Real system. (b) Idealized system. The isolation of primary and secondary circuit does not influence the basic system behavior and, therefore, is omitted in (b).

TABLE I
SWITCHING STATES OF THE PROPOSED SYSTEM AND RELATED VOLTAGE SPACE VECTORS $\underline{u}_{U,j}$ AND SIGNS $\text{sign}\{u_{T,1}\}$ OF THE TRANSFORMER PRIMARY VOLTAGE $u_{T,1}$ FOR $i_{N,R}>0$ AND $i_{N,S}, i_{N,T}<0$ AND/OR $\varphi_N \in (-(\pi/6), +(\pi/6))$

s_R	s_S	s_T	s_+	s_-	$\underline{u}_{U,j}$	$\text{sign}\{u_{T,1}\}$
0	0	0	1	1	0	0
0	0	1	1	1	0	0
0	1	0	1	1	0	0
0	1	1	1	0	$\frac{2}{3}\frac{N_1}{N_2}U_O$	−
1	0	0	0	1	$\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	0	1	0	1	$-\underline{a}\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	1	0	0	1	$-\underline{a}^2\frac{2}{3}\frac{N_1}{N_2}U_O$	+
1	1	1	0	0	0	±

order to guarantee a continuous flow of the phase currents $i_{N,i}$ (which are impressed by the mains-side inductances L) via $D_{F+,i}$ and S_+ or D_{F-} and S_-.

Based on this consideration, the switching-state combinations compiled in Table I and/or the system conduction states shown in Fig. 5 result.

Besides the possible switching states, we also have given in Table I the respective voltage space vectors $\underline{u}_{U,j}$ and the resulting signs $\text{sign}\{u_{T,1}\}$ of the transformer primary voltage $u_{T,1}$, e.g., for $s_R=1, s_S=0, s_T=0, s_+=0, s_-=1$, $i_{N,R}$ flows in positive direction in N_1. The current loop is closed via S_- and diodes $D_{F-,S}$ and $D_{F-,T}$ as phase currents $i_{N,S}$ and $i_{N,T}$. Due to $i_{T,1}=i_{N,R}>0$, there results a current $i_{T,2}=(N_2/N_1)i_{N,R}$ at the transformer output via

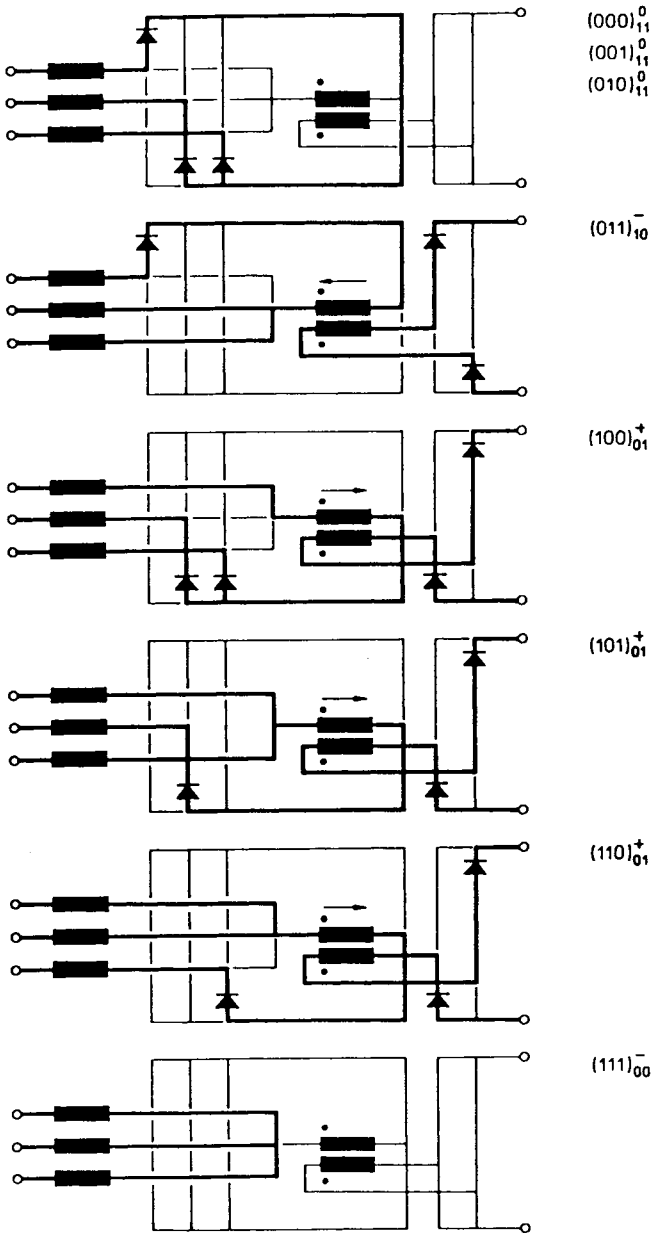


Fig. 5. Conduction states of the VIENNA Rectifier II for the possible switching states j according to Table I (valid for $i_{N,R}>0, i_{N,S}, i_{N,T}<0$). For the sake of clearness, the on states are shown for the circuit according to Fig. 2(d), for which the connections of the phase switching elements S_R, S_S, and S_T with the primary winding N_1 of the transformer are realized separately for each phase.

D_{22+} and D_{21-} and the output voltage U_O. Therefore, on the primary, a voltage $u_{T,1}=+(N_1/N_2)U_O$ ($\text{sign}\{u_{T,1}\}=+$) results and/or the rectifier input phase voltages related to a ficticious center tap of the winding N_1 have the values $u_{U,R}=+(1/2)(N_1/N_2)U_O$, $u_{U,S}=-(1/2)(N_1/N_2)U_O$ and $u_{U,T}=-(1/2)(N_1/N_2)U_O$. Therefore, according to (4), a space vector $\underline{u}_{U,(100)^+_{01}}=(2/3)(N_1/N_2)U_O$ is formed at the input of the rectifier system. For $j=(110)^+_{(01)}$ and $(101)^+_{01}$, there results a positive current $i_{T,1}=-i_{N,T}$ and/or $i_{T,1}=-i_{N,S}$ due to $|i_{N,R}|>|i_{N,S}|$ and/or $|i_{N,R}|>|i_{N,T}|$ and, therefore, a positive sign $\text{sign}\{u_{T,1}\}=+$ of the primary

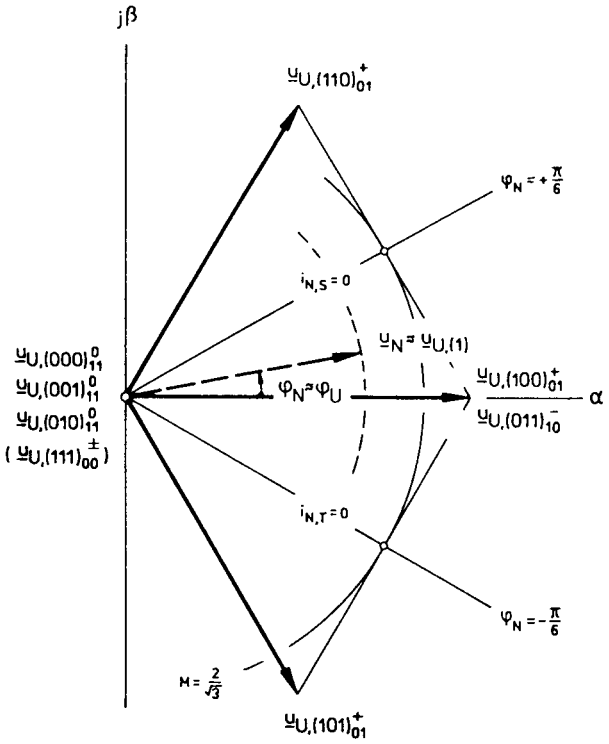


Fig. 6. Space vectors $\underline{u}_{U,j}$ of the input voltage associated with the switching states j of the PWM rectifier system according to Table I (based on $i_{N,R} > 0, i_{N,S}, i_{N,T} < 0$ and/or for $\varphi_N \in (-(\pi/6), +(\pi/6))$).

voltage $u_{T,1}$. Therefore, as mentioned at the beginning of this paper, also the orders of magnitude (besides the signs) of the phase currents take influence on the voltage generation.

Fig. 6 shows the complete set of the voltage space vectors resulting for the different switching states j which lie symmetrically around the angle interval $\varphi_N \in (-(\pi/6), +(\pi/6))$ of the current space vector $\underline{i}_N$ being associated with $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$.

For $s_+ = s_- = 1$ $((s_R s_S s_T) = (000)$ or (001) or (010)) and $s_R = s_S = s_T = 1$ $(s_+ s_- = 00)$ for $\varphi_N \in (-(\pi/6), +(\pi/6))$, there follows $\underline{u}_{U,j} = 0$; therefore, these switching states do represent nonactive or freewheeling states of the converter. Besides the switching state combination $s_+ s_- = 00$ shown in Table I, one can basically also set $s_+ s_- = 01$, 10, or 11 for $s_R = s_S = s_T = 1$ because, for the current flow on the mains side, a closed path via S_R, S_S, and S_T always exists. The specific choice of $s_+ s_-$ does not have any influence on the voltage generation at the input side of the rectifier system. However, the change of the magnetizing state of the transformer is influenced by $s_+ s_-$, as will be explained in more detail in Section IV-B. In this respect, the redundancy of the switching states $j = (100)^+_{(01)}$ and $(011)^-_{(10)}$ concerning voltage generation $\underline{u}_{U,j}$ is also of special importance.

IV. Mains Current Control and Transformer Volt-Second Balancing

A. Mains Current Control

For a sinusoidal shape of the mains current, one has to form a fundamental [designated by an index (1)] $\underline{u}_{U,(1)}$ of the rectifier input voltage by a current control in such a way that, in connection with the mains voltage, a current space vector $\underline{i}_N$ [see (3)] lying in phase with $\underline{u}_N$ results

$$\underline{u}_{U,(1)} = \underline{u}_N - j\omega_N L \underline{i}_N. \tag{5}$$

The fundamental voltage drop $j\omega_N L \underline{i}_N$ resulting across the mains-side series inductances L can be neglected in a first approximation for high switching frequencies $f_P \gg f_N$ (and/or small inductances L). Therefore, for the further considerations

$$\underline{u}_{U,(1)} = \hat{U}_{U,(1)} \exp j\varphi_U \approx \underline{u}_N = \hat{U}_N \exp j\varphi_N \tag{6}$$

is assumed. Therefore, full system controllability is linked to a minimum output voltage value

$$U_O > \frac{N_2}{N_1}\sqrt{3}\hat{U}_N. \tag{7}$$

As shown in Fig. 6, we have for the generation of $\underline{u}_{U,(1)}$ (in the average over a pulse half period) for each sign combination of the phase currents space vectors $\underline{u}_{U,j}$ lying symmetrically around the center axis of the possible positions of the current space vector $\underline{i}_N$ [and/or of $\underline{u}_{U,(1)}$ or $\underline{u}_N$, see (3) and (6)]. For a minimum ripple of the phase currents, only space vectors $\underline{u}_{U,j}$ lying in the immediate neighborhood of $\underline{u}_{U,(1)}$ are incorporated into the switching state sequence of a pulse period. With regard to a switching loss minimization, they are arranged in such a manner that the transition to the respective following switching state requires the switching of only one phase (and, possibly, of one of the switches S_+ or S_-). Now, for the position of $\underline{u}_{U,(1)} \approx \underline{u}_N$ shown in Fig. 6, there results the switching-state sequence

$$\begin{aligned}\cdots|_{t_\mu=0}(100)^+_{01} \rightarrow (110)^+_{01} \rightarrow (111)^0_{11} \rightarrow (011)^-_{10}|_{t_\mu=(1/2)T_P}\\ (011)^-_{10} \rightarrow (111)^0_{11} \rightarrow (110)^+_{01} \rightarrow (100)^+_{01}|_{t_\mu=T_P}\cdots.\end{aligned} \tag{8}$$

(t_μ denotes a local time being counted within a pulse period T_P). The relative on time δ_j of the switching states j can be calculated considering Fig. 6 and considering the relation

$$\underline{u}_{U,(1)} = \delta_{(110)^+_{01}} \underline{u}_{U,(110)^+_{01}} + (\delta_{(100)^+_{01}} + \delta_{(011)^-_{10}})\, \underline{u}_{U,(100)^+_{01}} \tag{9}$$

which is obtained by integration

$$\underline{u}_{U,(1)} = \frac{1}{T_P} \int_{T_P} \underline{u}_{U,j}\{t_\mu\}\, dt_\mu$$

of the different space vectors $\underline{u}_{U,j}\{t_\mu\}$ to the average voltage generation $\underline{u}_{U,(1)}$ within a pulse half period; with (9), (6), Table I, and (4), one receives

$$\begin{aligned}\delta_{(110)^+_{01}} &= \frac{\sqrt{3}}{2} M \sin(\varphi_U)\\ \delta_{(100)^+_{01}} + \delta_{(011)^-_{10}} &= \frac{\sqrt{3}}{2} M \sin\left(\frac{\pi}{3} - \varphi_U\right)\\ \delta_{(111)^0_{11}} &= 1 - (\delta_{(110)^+_{01}} + \delta_{(100)^+_{01}} + \delta_{(011)^-_{10}})\end{aligned} \tag{10}$$

[$\varphi_U \approx \varphi_N$, see (6)]. There,

$$M = \frac{\hat{U}_{U,(1)}}{\frac{1}{2}\frac{N_1}{N_2}U_O} \tag{11}$$

designates the modulation depth $M \in (0,(2/\sqrt{3}))$ of the system.

By the switching states $(100)^+_{01}$ and $(011)^-_{10}$, identical space vectors $\underline{u}_{U,(100)^+_{01}} = \underline{u}_{U,(011)^-_{10}}$ are formed (see Fig. 6). However, there result transformer primary voltages with inverse signs, as denoted by the indexes. This existing redundancy concerning voltage formation can (as shown in the following) be used for obtaining a purely alternating transformer magnetization with switching frequency.

B. Transformer Volt-Second Balancing

In order to avoid the occurrence of low-frequency components of the transformer primary voltage, one has to basically generate an equilibrium of the positive and negative volt seconds resulting within each pulse half period across the transformer primary (and/or secondary). Related to the switching-state sequence (8) as considered here, this leads to the relation

$$\delta_{(100)^+_{01}} + \delta_{(110)^+_{01}} = \delta_{(011)^-_{10}}. \tag{12}$$

Thereby, in connection with (10), one receives for the relative on time of the redundant switching states

$$\begin{aligned}\delta_{(100)^+_{01}} &= \frac{3}{4}M\sin\left(\frac{\pi}{6} - \varphi_U\right)\\ \delta_{(011)^-_{10}} &= \frac{3}{4}M\sin\left(\varphi_U + \frac{\pi}{3}\right).\end{aligned} \tag{13}$$

It is important to point out that—so far—always the switching state $(111)^0_{11}$ and not the switching state $(111)^{\pm}_{00}$ given in Table I has been incorporated into the switching-state sequence considered. For $s_+s_- = 11$, one has (independently of s_R, s_S, s_T) a short circuit of the primary leading via the diodes $D_{M+,i}$, $D_{F+,i}$, and S_+ or $D_{M-,i}$, $D_{F-,i}$, and S_-. Therefore, the secondary remains without current. The mains current is fed partially via S_R, S_S, and S_T and partially via S_+ and S_-. There, the specific current distribution is determined by the forward voltage drop of the valves. The magnetizing state $i_m = (1/L_m)\int u_{T,1}\,dt$ of the transformer is not changed (according to the neglection of the winding resistances and of the valves forward voltage drops). The magnetizing current path is leading for $i_m > 0$ via S_- and the diodes $D_{F-,i}$ and $D_{M-,i}$, for $i_m < 0$ via S_+ and $D_{F+,i}$ and $D_{M+,i}$.

As opposed to this, the magnetizing current for $s_+s_- = 00$ $(s_R = s_S = s_T = 1)$ is conducted only on the secondary of the transformer and, therefore, is decreasing $(i_m(N_1/N_2) \rightarrow 0)$ according to the secondary voltage. On the primary, then, there is no closed current path for i_m; i_m then has, possibly, a discontinuous shape because the output diodes do not allow a current sign reversal. The mains currents have freewheeling paths via S_R, S_S, and S_T. The sign of $u_{T,1}$ in this case is dependent on the sign of $i_m(N_1/N_2)$ and can be positive or negative; accordingly, $\text{sign}\{u_{T,1}\} = \pm$ is given in Table I).

Therefore, besides the distribution of the relative on times of the switching states $(100)^+_{01}$ and $(011)^-_{10}$, one could also influence the transformer magnetization via an appropriate choice of the freewheeling states. For the sake of brevity, this will not be treated in more detail here. Only the transformer operation with continuous magnetizing current shape is analyzed and/or only $(111)^0_{(11)}$ is taken as the freewheeling state.

Remark: As mentioned in Section III-A, the power semiconductors are assumed ideal in this paper and, also, the transformer winding resistances are neglected. For a detailed analysis of the magnetization, one would have to consider these parasitic quantities, however, similar to the analysis of a push–pull center-tapped dc-to-dc converter in [30]. The magnetizing acting voltage is then dependent not only on the sign, but (to a minor extent) also on the actual value of the primary and secondary current.

The control method considered so far can be realized in a simple way by a ramp-comparison current controller (see [31] or [32, Fig. 14]) in connection with a direct control of the mains phase currents (see Fig. 8). As shown in Fig. 8(b), then the switching instants of the power transistors S_i are determined via the intersection of the sum of the current control error $\Delta i_{N,i}$ (dynamically weighted by a current controller $G(s)$) and a precontrol signal m_i. There, one has to consider the dependency of the voltage generation $u_{U,i}$ (mentioned in Section III-B) on the sign of the associated phase current $i_{N,i}$ by inversion

$$s_i = \begin{cases} s_i', & \text{if } i^*_{N,i} \geq 0 \\ \text{NOT } s_i', & \text{if } i^*_{N,i} < 0 \end{cases} \tag{14}$$

of the switching decision

$$s_i' = \begin{cases} 0, & \text{if } i_D < m_i - \Delta i_{N,i} \\ 1, & \text{if } i_D > m_i - \Delta i_{N,i} \end{cases} \tag{15}$$

of the pulsewidth modulator for $i_{N,i} \approx i^*_{N,i} < 0$; there $\Delta i_{N,i} = i^*_{N,i} - i_{N,i}$, $i^*_{N,i}$ denotes the phase current reference value.

By the precontrol signals m_i, the following shall be obtained.

- There shall be obtained the distribution of the switching states which are redundant with respect to the voltage generation (between the begin and end of each pulse half interval) required for a symmetric transformer magnetization.
- For $\Delta i_{N,i} = 0$ at the system input a voltage having a fundamental $\underline{u}_{U,(1)}$ equal to the mains voltage $\underline{u}_N$ shall be formed. Then, the current controller has to provide only the relatively small fundamental voltage drop across the series inductors L. Furthermore, despite the fact that the gain of an integrally acting component of $G(s)$ is limited to finite values for mains frequency variations, the control error is limited to small values (see [33, Fig. 22]).

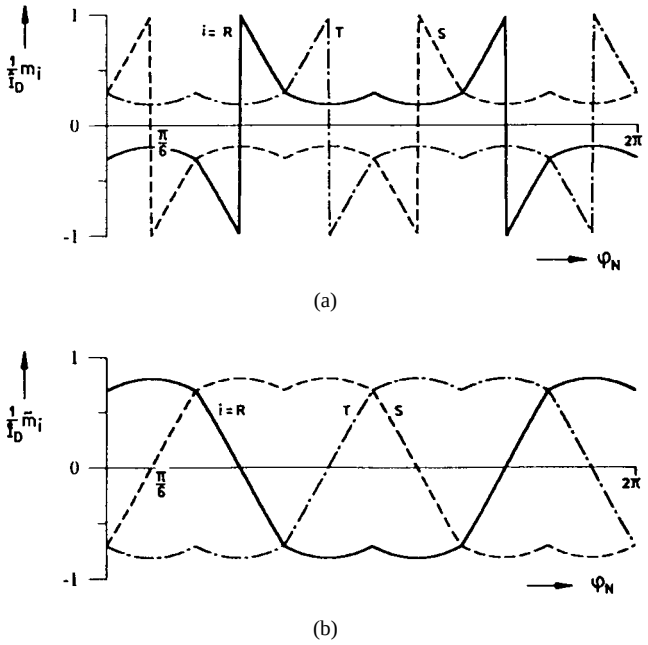


Fig. 7. Shape of the precontrol signals m_i of the ramp-comparison control within a mains period [see (a)] rated with respect to $\hat{I}_D$. The continuous shape $\tilde{m}_i$ of the precontrol signals as shown in (b) can be obtained based on (a) by addition of rectangular signals according to (17).

The signal shape

$$\varphi_U \in \left(0, +\frac{\pi}{6}\right): \quad \begin{aligned} m_R &= \frac{\sqrt{3}}{2} M \hat{I}_D \sin\left(\varphi_U + \frac{\pi}{3}\right) - \hat{I}_D \\ m_S &= \hat{I}_D - \frac{3}{2} M \hat{I}_D \sin\left(\frac{\pi}{6} - \varphi_U\right) \\ m_T &= \hat{I}_D - \frac{\sqrt{3}}{2} M \hat{I}_D \sin\left(\varphi_U + \frac{\pi}{3}\right) \end{aligned} \tag{16}$$

being directly calculable based on (10) and (12) (the shape in the other intervals of the mains period follows simply by symmetry considerations) is shown in Fig. 7(a). For the sake of brevity, a more detailed description of the derivation of (16) is omitted here. We only want to point out that by subtraction

$$\tilde{m}_i = \begin{cases} m_i - \hat{I}_D, & \text{if } m_i \geq 0 \\ m_i + \hat{I}_D, & \text{if } m_i < 0 \end{cases} \tag{17}$$

of a rectangular function (defined via the sign of m_i and/or of $u_{N,i}$) of the amplitude $\hat{I}_D$ a continuous shape $\tilde{m}_i$ of the precontrol signals can be obtained [see Fig. 7(b)]. Surprisingly, thereby a signal shape results which is known from the modulation functions for space-vector modulation for bidirectional six-switch boost-type voltage dc-link PWM rectifier systems (see Fig. 7(b) and [34, Fig. 12]).

C. Overall Structure of the System Control

The block diagram of a two-loop system control with output voltage controller as master control and ramp-comparison current control as slave control is shown in Fig. 8.

The phase current reference values $i^*_{N,i}$ have a shape proportional to the associated mains phase voltages $u_{N,i}$ (resistive fundamental mains behavior). The reference value of the amplitude $\hat{I}^*_N$ of the mains phase currents is set by the output voltage controller $F(s)$ in dependency on the control error of the output voltage $u^*_O - u_O$. As described in Section IV-B, the influence of the mains phase voltages on the current control is compensated by precontrol signals m_i, which also guarantee a symmetric magnetization of the transformer magnetic core. Based on the switching decisions s'_i of the modulator stage of the current controller, the phase switching functions s_R, s_S, and s_T are generated according to (14) as well as the related switching states $s_+ s_-$ being formed by a combinatorial logic circuit according to Table I. There, as mentioned before, the freewheeling state is represented by $(111)^0_{11}$ and not by $(111)^{\pm}_{00}$. Into the combinatorial logic, the correction (as described in Section IV-D) of dynamically occurring erroneous switching states of the current controller is also included.

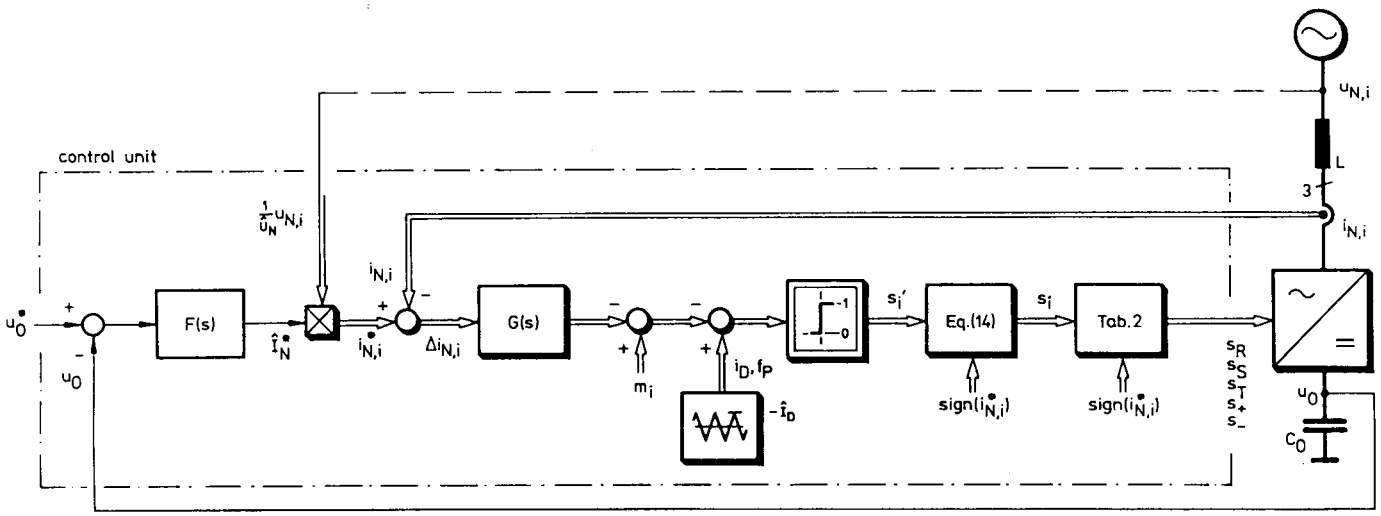
Fig. 8 shows the derivation of the phase switching functions s_i via intersection of the triangular carrier wave i_D with the precontrol signals m_i for stationary operation and for one pulse period T_P. If, e.g., the current control error $\Delta i_{N,R} = +\Delta i_N$, $\Delta i_{N,S} = \Delta i_{N,T} = -(1/2)\Delta i_N$ occurs (as shown by dashed lines), the relative on time of the switching state $(111)^0_{(11)}$ is increased and the relative on time of the switching states $(100)^+_{(01)}$ and $(011)^-_{(10)}$ is reduced accordingly. This leads to an increase of the absolute value i_N of the mains current space vector by $\underline{u}_N$ ($L(d\underline{i}_N/dt) = \underline{u}_N - \underline{u}_{U,(111)^0_{11}}$, $\underline{u}_{U,(111)^0_{11}} = 0$), eliminating the control error Δi_N.

Remark: In Fig. 8(b), the signals $\Delta i_{N,i}$ are shown constant over T_P for a clear representation; in reality, however, a variation in the control errors will take place due to the changes of the system switching state.

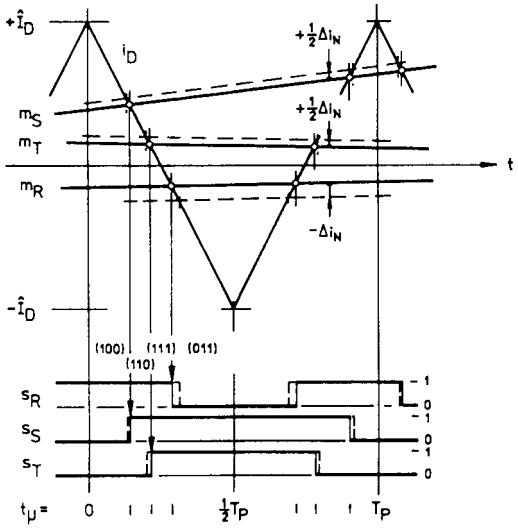
D. Correction of Dynamically Occurring False Switching Decisions of the Current Controller

According to (8), within the angle interval $\varphi_N \in (0, +(\pi/6))$ (considered in connection with Fig. 6) in the stationary case, only switching states $(s_R s_S s_T) = (100), (110), (111), (011)$ and in $\varphi_N \in (-(\pi/6), 0)$ only (100), (101), (111), (011) are applied for voltage generation. The switching states remaining in comparison to Table I result only for the dynamic case (as a more detailed analysis of the selected current control concept shows), e.g., for a high step change of the reference value $\hat{I}^*_N$ of the mains current amplitude.

If, e.g., based on the relations shown in Fig. 8(b), the tip of the mains current space vector $\underline{i}_N$ shall be guided by $\Delta\underline{i}_N$ in the direction of the negative phase axis R and/or the absolute value i_N of $\underline{i}_N$ shall be reduced, then the switching state $(000)^0_{11}$ and/or $\underline{u}_{U,(000)^0_{11}}$ is generated by the current controller for sufficiently large Δi_N. (For $\Delta\underline{i}_N = \Delta i_{N,R} < 0$ there follows $\Delta i_{N,S} = \Delta i_{N,T} = -(1/2)\Delta i_{N,R} > 0$ due to $\Delta i_{N,R} + \Delta i_{N,S} + \Delta i_{N,T} = 0$.) Due to the mains voltage $\underline{u}_N$ there would result an *increase*, however, and not a decrease of i_N, which has to be avoided by recoding of $(000)^0_{11}$ in $(100)^+_{01}$ or $(011)^-_{10}$ (see Table II).



(a)



(b)

Fig. 8. Block diagram of the two-loop control [see (a)] of the VIENNA Rectifier II (shown schematically); for the sake of clearness, signal paths being equal for all phases are combined in double lines. (b) Time behavior of the triangular carrier wave i_D of the ramp-comparison current controller, of the precontrol signals m_i, of a superimposed current control error $\Delta i_{N,R} = +\Delta i_N$, $\Delta i_{N,S} = \Delta i_{N,T} = -(1/2)\Delta i_N$, and of the control signals s_i generated within a pulse period T_P.

TABLE II
CORRECTION OF THE DYNAMICALLY OCCURRING FALSE SWITCHING DECISIONS OF THE CURRENT CONTROLLER FOR $\varphi_N \in (-(\pi/6), +(\pi/6))$

controller output		applied switching state
$(000)^0_{11}$	→	$(100)^+_{01}$ or $(011)^-_{10}$
$(001)^0_{11}$	→	$(101)^+_{01}$
$(010)^0_{11}$	→	$(110)^+_{01}$

The further corrections of false switching decisions given in Table II could be derived in a similar manner by assuming a step change of $\underline{i}_N$ in positive direction of the phase axis $S, \Delta\underline{i}_N = \Delta i_{N,S} > 0$, $\Delta i_{N,R} = \Delta i_{N,T} = -(1/2)\Delta i_{N,S} < 0$, and/or the phase axis $T, \Delta\underline{i}_N = \Delta i_{N,T} > 0$, $\Delta i_{N,R} = \Delta i_{N,S} = -(1/2)\Delta i_{N,T} < 0$.

In general, the switching states corresponding to a false switching decision of the current controller are determined by the signs of the phase currents. The corrections to be taken for the $\pi/3$-wide intervals of the mains period not treated here can simply be derived by considerations analogous to the considerations described so far. For the sake of brevity, a more detailed discussion shall be omitted here.

V. SIMULATION RESULTS

The theoretical considerations of the previous sections have been verified by digital simulation for the following operating parameters (which are typical for a system application such as a high-power telecommunications power supply module):

$$U_{N,\mathrm{rms}} = 230\ \mathrm{V}, \qquad f_N = 50\ \mathrm{Hz}$$
$$\frac{N_1}{N_2}U_O = 700\ \mathrm{V}, \qquad L = 1\ \mathrm{mH}$$
$$\hat{I}_N = 18\ \mathrm{A}, \qquad L_m = 5\ \mathrm{mH}.$$

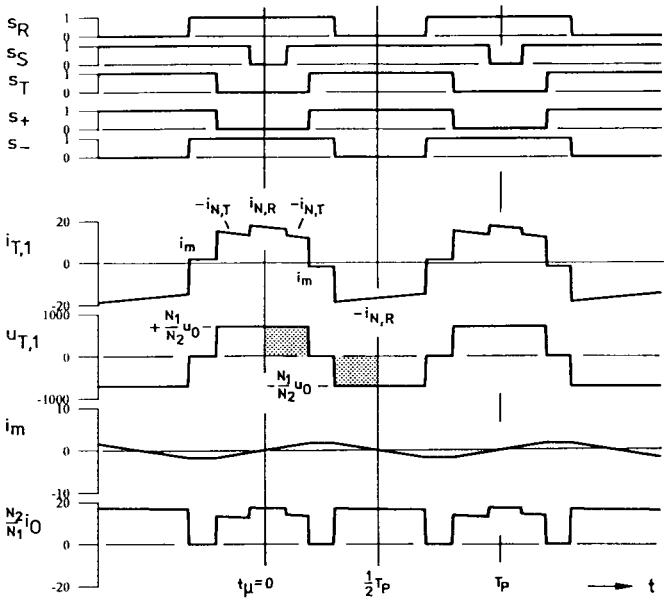


Fig. 9. Detail of the time behavior of the control signals s_i, s_+, and s_-, of the transformer primary current $i_{T,1}$, of the transformer primary voltage $u_{T,1}$, of the magnetizing current i_m, and of the transformed output current $(N_2/N_1)i_O$ for $\varphi_N \approx (\pi/12)$ $(i_{N,R} > 0, i_{N_S} < 0, i_{N,T} < 0)$.

The switching frequency has been set to $f_P = 16$ kHz under consideration of the duration of a simulation run. For a practical realization and for the requirement of high power density, f_P would have to be selected higher by at least a factor of 2 (reduction of the inductances L and L_m being relatively high in the case at hand). Thereby, however, in general, a reduced efficiency of the energy transformation results due to the higher switching losses. For the sake of brevity, $G(s)$ has been set to 1 and/or the output voltage has been assumed impressed. Therefore, the dimensioning of the output voltage controller $F(s)$ could be omitted. The triangular carrier wave i_D has been set to $\hat{I}_D = 10$ A.

Based on the parameters previously compiled, the modulation depth according to (11) follows as:

$$M = 0.934.$$

Thereby, a sufficiently large distance from the modulation limit $M = (2/\sqrt{3}) \approx 1.15$ is guaranteed and high control dynamics is given. The simulation results are shown in Figs. 9 and 10.

Fig. 9 shows a detail of the shape of the phase switching functions s_i, $i = R, S, T$, and of the control signals s_+ and s_-. Furthermore, the transformer primary current $i_{T,1}$ formed from mains phase current sections and the resulting transformer primary voltage $u_{T,1}$ are shown. The equilibrium of the positive and negative volt seconds across the transformer (which is pointed out in Fig. 9 for a pulse half period by dotted areas) and/or the symmetric magnetization of the transformer magnetic core becomes clear via the shape of the magnetizing current i_m. A change of i_m results only for the active switching states $(100)^+_{01}$, $(110)^+_{01}$, and $(011)^-_{10}$; for freewheeling $(111)^0_{11}$ i_m remains constant due to the then given short circuit of the primary winding. The shape of the secondary current $(N_2/N_1)i_O$ can be derived from $i_{T,1}$ by subtraction of the magnetizing current and rectification [see Fig. 4(b)].

In Fig. 10(a), the shapes of the currents and voltages on the primary and of the output current within a mains period are shown. One has to point out there that, in particular, the system current consumption is almost purely sinusoidal (in phase with the mains voltage) despite the simple current control concept used. After filtering out the harmonics with switching frequency, this results in an approximately constant power flow to the output. The low-frequency harmonics existing in the spectrum of the mains phase current and of the output current [see Fig. 10(b)] now have very small amplitudes related to the fundamental $\hat{I}_N$ and/or to the average value $I_O = (3/2)(\hat{U}_N \hat{I}_N / U_O)$ [suppressed in Fig. 10(b)].

VI. Experimental Analysis

A first experimental analysis of the proposed system has been performed with a laboratory model (see Fig. 11) with a rated power of 2.5 kW, input line-to-line voltage $\sqrt{3}U_{N,\mathrm{rms}} =$ 110 V, and dc output voltage $U_O = 48$ V (according to the typical voltage level for telecommunications power suppies).

In order to keep the influence of parasitic capacitances and inductances on the system behavior low, a switching frequency of $f_P = 20$ kHz has been chosen, lying barely above the audible range. This makes possible the characterization of the conditions also for systems of higher power and with the application of IGBT's if high efficiency of the power conversion (low switching losses) is required.

A. Power Circuit Components

1) Power Semiconductors: The power transistors S_i, S_+ and S_- are realized by power MOSFET's IXYS IXFK 50N50 ($V_{\mathrm{DSS}} = 500$ V, $R_{\mathrm{DS(on)},T_j=25\,^\circ\mathrm{C}} = 0.1\,\Omega$). Because there do not exist special requirements concerning the reverse-recovery time of the valves $D_{N+,i}, D_{N-,i}, D_{M+,i}, D_{M-,i}$ [35], in each phase $i = R, S, T$, a single-phase bridge rectifier module SEMIKRON SKB26/08 ($V_{\mathrm{RRM}} = 800$ V, $I_{\mathrm{D}} = 18$ A) has been applied in place of discrete devices. Only for $D_{F+,i}$ and $D_{F-,i}$ diodes with very short reverse-recovery time (HARRIS RHRP 1560, $V_{\mathrm{RRM}} = 600$ V, $I_{\mathrm{F(AV)}} = 15$ A, $t_{\mathrm{rr}} = 40$ ns) have been provided. The secondary rectification has been performed by Schottky diodes IR 40CPQ060 ($V_{\mathrm{RRM}} = 60$ V, $I_{\mathrm{F(AV)}} = 40$ A), where each of the valves D_{21+}, D_{21-}, D_{22+}, D_{22-} has been realized by paralleling of the two diodes incorporated in the same package. At present, the realization of the secondary side as a center-tapped circuit (being advantageous regarding low conduction losses) has been omitted with respect to a construction of the transformer as simply as possible.

For damping of parasitic oscillations between parasitic inductances and output capacitances, *RC* snubbers have been provided across all power transistors. Furthermore, for the limitation of switching overvoltages across the power semiconductors on the primary a low-loss overvoltage limiting circuit (see Section VI-C and Fig. 11) has been provided.

2) Input Inductors and Transformer: The input inductances $L = 500$ μH have been realized (with regard to low

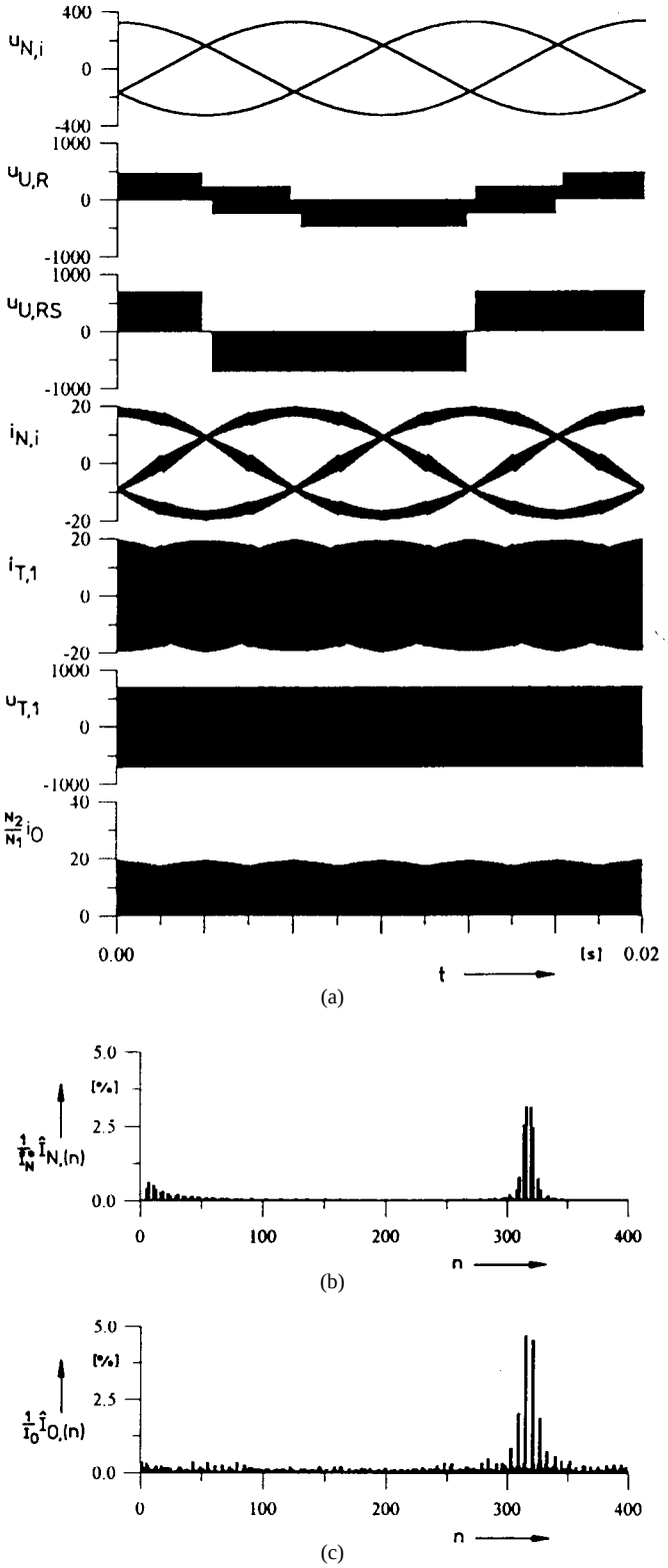


Fig. 10. Digital simulation of the time behavior of the mains phase voltages $u_{N,i}, i = R, S, T$, of the line-to-line rectifier input voltage $u_{U,RS}$, of the rectifier input phase voltage $u_{U,R}$ related to the mains star point N, of the mains phase currents $i_{N,i}$, of the transformer primary current $i_{T,1}$, of the transformer primary voltage $u_{T,1}$, and of the load current i_O within a mains period [see (a)]. Also shown are the rated spectrum of the mains current [see (b), fundamental component $\hat{I}_N$ suppressed] and of the output current i_O [see (c), dc value I_O suppressed; *remark*: harmonics with higher amplitudes are concentrated in the vicinity of multiples of $2f_P$, i.e., $n = 600$, 1200, etc.]. n denotes the order of the harmonics related to the mains frequency f_N.

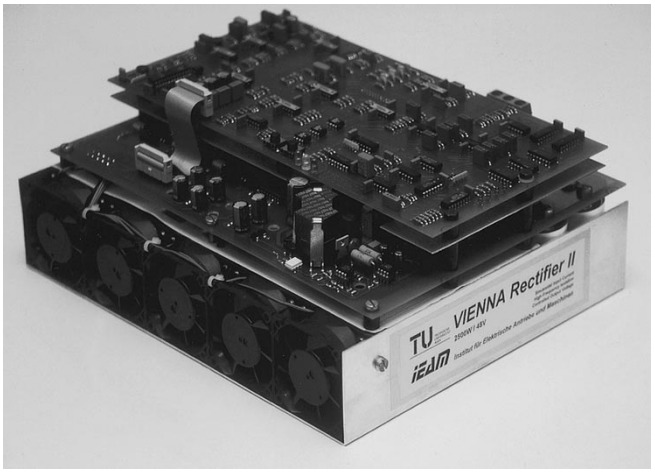


Fig. 11. 2.5-kW laboratory model of the VIENNA Rectifier II. Dimensions: 30 cm × 26 cm × 11 cm (11.8 in × 10.2 in × 4.3 in). The control circuit board is located horizontally above the power print. The transformer (ferrite core SIEMENS RM 14) of the flyback converter for controlling the limitation voltage and for power supply for control electronics and fans is visible in the foreground.

core losses and realization cost) with ferrite cores SIEMENS E65 and HF litz wire 350 × 0.1 CuL ($N = 59$; saturation current, 25 A) and the high-frequency transformer with the same core and split primary winding ($N_1 = 2 \times 12$; HF litz wire 420 × 0.1 CuL), lying on both sides of the secondary winding ($N_2 = 6$; three foils 0.1 mm/35 mm in parallel). For a primary inductance $L_m = 4.6$ mH, a very low stray factor $(L_\sigma/L_m) = 0.006$ could be realized by this construction. By a turns ratio $(N_1/N_2) = 6$ in connection with the given input and output voltages, a stationary value of $M \approx 0.936$ has been set, approximately equal to the modulation depth selected in Section V.

3) Output Capacitor: The output capacitor C_O has been selected based on the relatively high current stress ($I_{C_O,\mathrm{rms}} = 0.75 I_O$, see Section VI-E) due to the discontinuous output current by four electrolytic capacitors EVOX-RIFA PEH 4700 μF/63 V (maximum allowable current carrying capability: $I_{\mathrm{RAC},40\,^\circ\mathrm{C},10\,\mathrm{kHz}} = 18$ A) in parallel.

4) Mechanical Construction: The low-inductance connections of the power devices have been achieved (as shown in Fig. 11) by a power print (70-μ copper thickness) being situated directly above the heat sink FISCHER SK 56-150 ($R_{\mathrm{th}} = 0.34$ K/W); the input inductors, the high-frequency transformer, and the output capacitors have been mounted such that they are located in the stream of cooling air on the lower side of the printed circuit board.

B. Control Circuit

The control of the system has been realized in analog technology (see Fig. 11). As compared to a digital realization (as planned in the next step) with a microcontroller or digital signal processor (DSP), this has reduced the development effort. Also, the test of partial functions has been simplified.

1) Current Measurement and Control: For the input current measurement, two phase currents are sensed with current sensors 1:1000 (LEM Instruments, LA 25-NP); the third

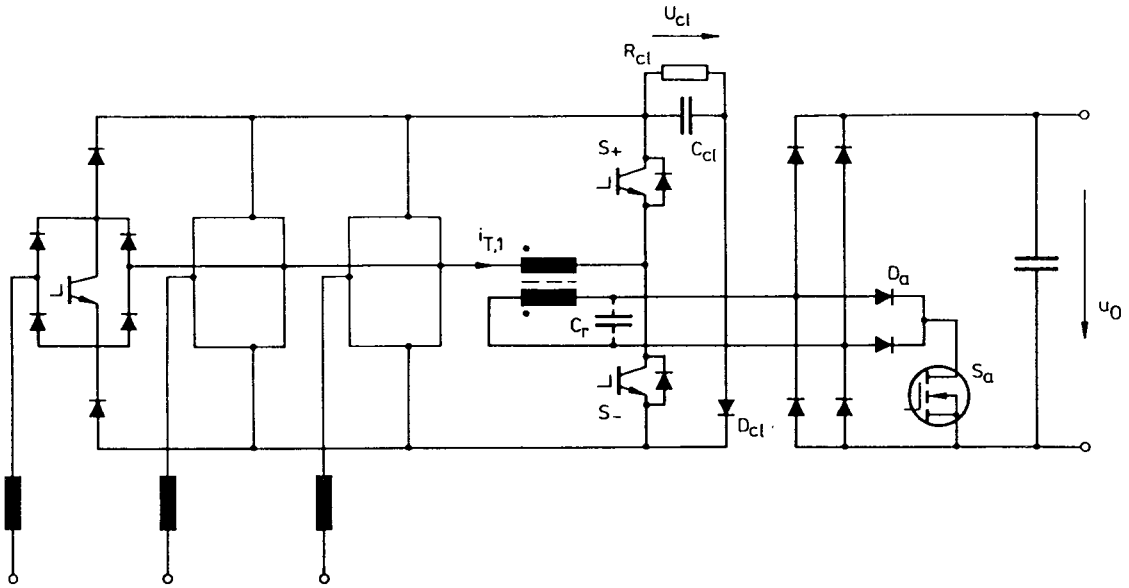


Fig. 12. Circuit measures for limiting the switching overvoltages occurring due to the transformer stray inductance. Due to the overvoltage limitation circuit D_{cl}, C_{cl}, R_{cl} the overvoltages (resulting for step changes of $i_{T,1}$) of all valves on the primary are limited to U_{cl}. A reduction of the limitation power can be obtained by an auxiliary switch S_a on the secondary. A basically lossless system operation is possible if one changes from hard- to soft-switching operation by connecting a capacitor C_r in parallel to the secondary.

phase current has been calculated according to the relationship $i_{N,R} + i_{N,S} + i_{N,T} = 0$ being valid due to the missing connection of the circuit with the mains star point. For a dimensioning of the control as simply as possible, the phase current controllers $G(s)$ have been realized as proportional (P) controllers; the output voltage controller $F(s)$ has been realized as a proportional integral (PI) controller with regard to stationary control accuracy.

The recoding of the output signals of the phase current controllers, i.e., the inversion of a switching decision s_i' for negative sign $\mathrm{sign}\{i^*_{N,i}\} = -$ of the related phase current reference value [see (14)] and the correction of false switching decisions according to Table II [see Fig. 8(a)] has been realized with a 2k-word by 8-bit CMOS electrically programmable read-only memory (EPROM) (CYPRESS CY7C291).

2) Precontrol Signals: The precontrol signals m_i have been composed by analog switches directly from segments of the mains phase voltages $u_{N,i}$ [which are measured for gaining the phase current reference values $i^*_{N,i} = (1/\hat{U}_N)u_{N,i}$, see Fig. 8(a)] and of the line-to-line mains voltages gained from the differences. This has given in all cases a matching of the precontrol to the actual mains voltage conditions with small realization effort.

3) Control of the Power Semiconductors: The transfer of the control energy has been achieved for each transistor separately by a small-signal common-mode filter inductor ($N_1 = N_2 = 80$ on ferrite core SIEMENS EP7) used as a high-frequency transformer. The control information has been transmitted via optocouplers (TOSHIBA TLP 250) with output driver stage having high common-mode transient immunity and a typical small-signal propagation delay time of $t_{\mathrm{pLH}} = t_{\mathrm{pHL}} = 150$ ns.

As has become clear during a detailed experimental investigation of the system, one can completely avoid turn-on and turn-off losses for the power transistors $S_i, i = R, S, T$, by an appropriate time shift of the switching state changes of S_+ and S_- as compared to the related switching state changes of S_i. Thereby, in S_+ and S_-, only turn-off losses result. Alternatively, a reduction of the switching losses can be achieved also by changing from hard- to soft-switching operation . Thereby, the stray inductance L_σ can be incorporated into the system function. For this, in analogy to [36, Fig. 4.16], one has to provide a capacitor C_r across the output terminals of the transformer. Furthermore, then the switching state sequence according to (8) has to be extended to $(100)^+_{01} \rightarrow (110)^+_{01} \rightarrow (111)^+_{00} \rightarrow (000)^+_{11} \rightarrow (011)^-_{10} \rightarrow (111)^-_{00} \rightarrow (000)^-_{11} \rightarrow (100)^+_{01}$. (Then, the magnetizing voltage is defined by C_r and, therefore, maintained also for blocking output diodes.) For the sake of brevity, a comparison of the two control methods shall be left to a future paper.

C. Overvoltage Limitation

A problem of the practical realization of the proposed circuit consists in the fact that the transformer is operated not as voltage-fed (as for a buck-derived converter system), but as current-fed. Naturally, thereby, every change of the switching state and/or of the transformer primary current is linked to the occurrence of an overvoltage. This overvoltage has to be limited by an overvoltage limitation circuit D_{cl}, U_{cl} (see Fig. 12), e.g., between the positive and negative primary voltage bus. Only by this approach can exceeding of the maximum allowable blocking voltage stress on the power semiconductors be avoided.

As the experimental analysis shows (and as can be verified by analytical calculations), the average power fed into the clamp circuit during switching processes shows a highly nonlinear dependency on the magnitude of the limiting voltage U_{cl} relative to the line-to-line mains voltage $\sqrt{3}\hat{U}_N$. For rated conditions, 2% of the output power P_O are delivered into the electrolytic capacitor $C_{cl} = 2 \times 68\ \mu$ for $U_{cl} = 300$ V. The respective values are 3.5% for $U_{cl} = 250$ V and 5% for $U_{cl} = 225$ V. With respect to high efficiency of the energy conversion, instead of the discharging resisitor R_{cl} (shown in Fig. 11), a flyback converter has been provided which is connected to the controlled output voltage u_O on the secondary; it transfers continuously the energy fed into C_{cl} in the form of pulses to the output (see [36, p. 152]). Furthermore, this dc-to-dc converter serves as a potential-free power supply for the control electronics (power consumption 20 W) and for feeding of the fans (power consumption 6 W). Also, it serves for the precharging of the output capacitor during system startup, as described in the following section.

Remark: One has to note that by a power transistor S_a (and decoupling diodes D_a) situated on the secondary, a significant reduction of the limitation power can be achieved. This has been proposed in [17] in connection with a single-switch three-phase flyback converter topology and also has been analyzed in [37]. By S_a, the secondary is shortened during changes of the primary current as forced by switching state changes of the system. Thereby, the full limitation voltage is available for obtaining of a new stationary current value which is delayed by the stray inductance and not only the difference of the limitation voltage and the voltage coupled into the transformer primary. The time interval for the current commutation is substantially shortened thereby and/or the power fed into the clamp circuit is substantially reduced.

D. System Startup and Overload Protection

As mentioned in [10], the startup and the overload protection (short circuit of the output voltage) represent critical operating conditions for a single-stage boost-derived converter system. In both cases, the voltage coupled into the transformer primary (which guides the mains current) is missing. The current being driven by the mains voltage cannot be limited, therefore, independently of the converter switching state, i.e., also for the active switching states $(100)_{01}, (011)_{10}$, $(110)_{01}$ and $(101)_{01}$ (in $\varphi_N \in (-(\pi/6), +(\pi/6))$) being voltage forming during regular operation. In case of a short circuit of the output voltage $(U_O = 0)$, one has to block, therefore, immediately all power transistors $(s_i, s_+, s_- \rightarrow 0)$. The energy stored in the mains side inductances is then fed into the limitation circuit U_{cl}; this has to be taken into consideration for dimensioning the storage capacitor C_{cl}. Then, finally, the phase currents $i_{N,i}$ become zero. Therefore, a limitation circuit is required also in such cases when no overvoltages result for regular operation (i.e., e.g., for soft-switching operation).

For the laboratory model, the clamp capacitor C_{cl} has been charged for blocked power transistors $(s_i = 0$ und $s_+ = s_- = 0)$ without an explicit precharge circuit via the diodes $D_{N+}, D_{F+}, D_{cl}, D_{F-}$, and D_{N-} to the peak value of the mains line-to-line voltage. Because, as mentioned before, also the supply voltages of the electronics are realized by the flyback converter (discharging the clamp capacitor for regular operation and functioning from $U_{cl} \approx 100$ V), then the output capacitor C_O is precharged without additional control effort to the required starting value. There, the voltage being present across C_O and/or the main secondary winding of the flyback converter can simply be given via the turns ratio of the windings feeding the electronics and of the main secondary winding.

If the voltage required for current control is available, then the output undervoltage detection enables the control and adds the load.

E. Experimental Results

Characteristic signal shapes of the stationary operation of the laboratory model are shown in Fig. 13.

As can been seen from Fig. 13(a) and (b), the mains current is guided proportional to the mains voltage in accordance with the theoretical considerations. (The deviation of the mains voltage from the ideal sinusoidal shape is caused by a high mains load from single-phase rectifiers with capacitive smoothing, e.g., in office electronics, copying machines, etc.) The measured shape of the phase voltage $u_{U,R}$ and of the line-to-line voltage $u_{U,RS}$ at the converter input check the results of the digital simulation of the circuit (see Fig. 10).

The deviation of the shape of the transformer primary voltage from the simulation (see Fig. 10) can be explained by the finite leakage inductance of the transformer, which, as mentioned in Section VI-C, leads to a triggering of the overvoltage clamp circuit and/or to overvoltage peaks with amplitude 300 V for each switching state change. The simulation has been based on a leakage-free transformer $L_\sigma = 0$; however, the basic system behavior is represented correctly despite this simplification.

In the rated operating point, the following stresses on the primary power transistors and diodes (related to the peak value $\hat{I}_N$ of the mains current fundamental) and on the output diodes and the output capacitor (related to the mean value I_O of the output current) have been measured (which can be used as a first system evaluation during a concept study):

$$I_{Si,\mathrm{avg}} = 0.33 \text{ p.u.}, \qquad I_{Si,\mathrm{rms}} = 0.46 \text{ p.u.}$$
$$I_{S+,\mathrm{avg}} = 0.46 \text{ p.u.}, \qquad I_{S+,\mathrm{rms}} = 0.6 \text{ p.u.}$$
$$I_{D_N,\mathrm{avg}} = 0.32 \text{ p.u.}, \qquad I_{D_N,\mathrm{rms}} = 0.5 \text{ p.u.}$$
$$I_{D_M,\mathrm{avg}} = 0.16 \text{ p.u.}, \qquad I_{D_M,\mathrm{rms}} = 0.32 \text{ p.u.}$$
$$I_{D_F,\mathrm{avg}} = 0.16 \text{ p.u.}, \qquad I_{D_F,\mathrm{rms}} = 0.32 \text{ p.u.}$$
$$I_{D_{21+},\mathrm{avg}} = 0.5 \text{ p.u.}, \qquad I_{D_{21+},\mathrm{rms}} = 0.88 \text{ p.u.}$$
$$I_{C_O,\mathrm{rms}} = 0.75 \text{ p.u.}$$

S_+ and S_- show identical stresses; the same is valid for the diodes D_{21+}, D_{21-}, D_{22+}, and D_{22-} on the secondary.

Therefore, a current stress on the power transistors S_i results which is relatively low in relation to the rms value and the

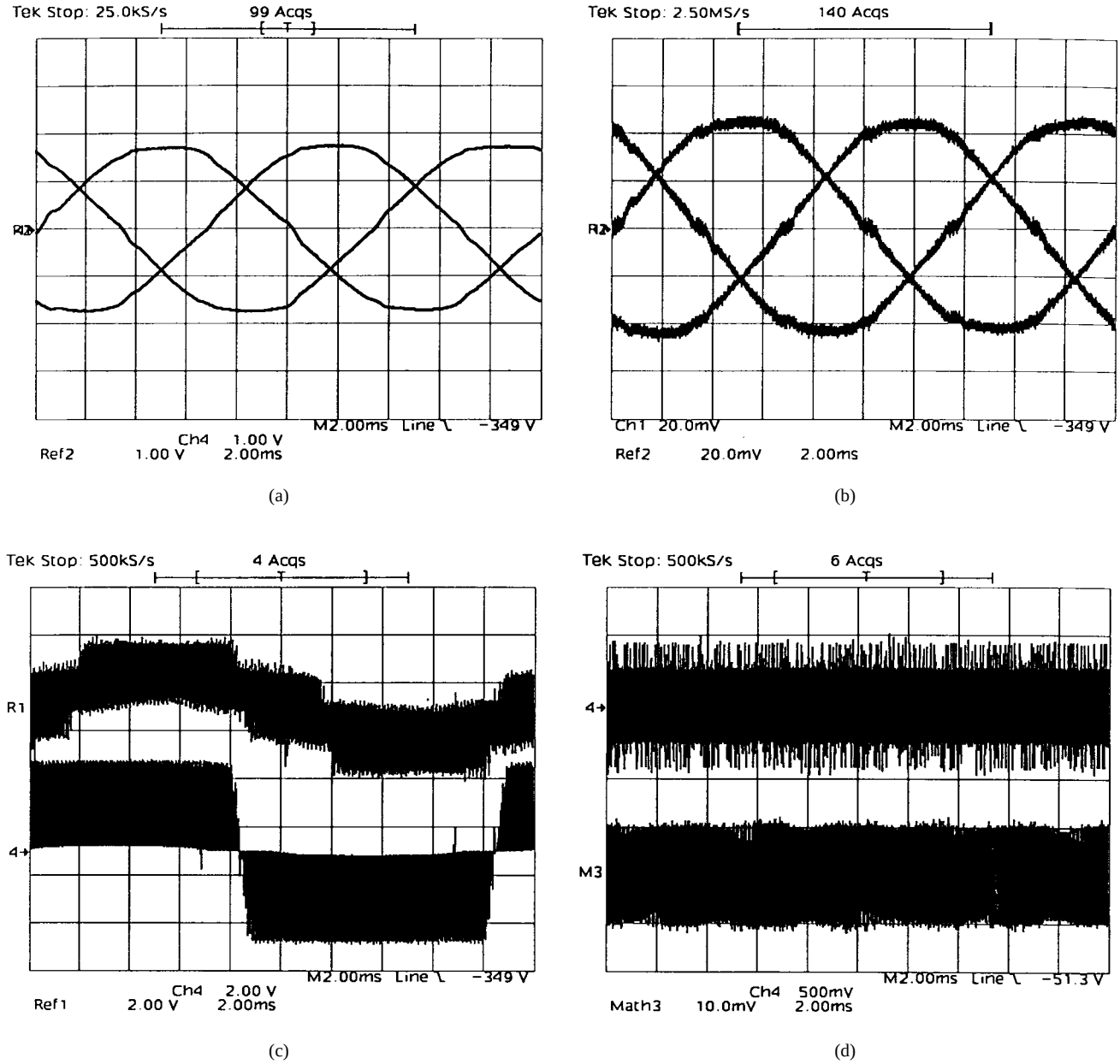


Fig. 13. Stationary operating behavior of the laboratory model, representation for one mains period. (a) Mains phase voltages $u_{N,R}, u_{N,S}$, and $u_{N,T}$ (50 V/div). (b) Mains phase currents $i_{N,R}, i_{N,S}$, and $i_{N,T}$ (10 A/div). (c) Phase voltage $u_{U,R}$ (related to the mains star point N) and line-to-line voltage $u_{U,RS}$ at the rectifier input (100 V/div). (d) Transformer primary voltage $u_{T,1}$ (250 V/div) and transformer primary current $i_{T,1}$ (20 A/div).

average absolute value of the mains current. For the values S_+ and S_- which are realized advantageously as an IGBT bridge half leg for higher input voltages, the rms current stress can be considered to be equal to the mains current rms value in a rough first approximation.

Due to space limitations, further results of the experimental analysis of the converter, as well as the approach for the dimensioning of the components, shall be compiled and discussed in a paper presently in preparation.

VII. Conclusions

In this paper, a novel topology of a single-stage three-phase ac-to-dc converter with sinusoidal input current shape and high-frequency isolation of the controlled output voltage has been proposed.

The system has (in particular, as compared to buck-derived topologies [38]) the following advantages and disadvantages. (The general advantages of single-stage as compared to two-stage converter systems, already mentioned in Section I, are not again discussed in detail here.)

The advantages are as follows.

- There is a simple structure of the power and control circuits (the control described can be realized in purely analog fashion).
- There is continuous sinusoidal input current shape (reduction of the filtering effort required on the mains side and/or lower electromagnetic influence on other systems).

- According to the constant power flow at the input for sinusoidal current shape, there are no low-frequency harmonics of the output current (low psophometric noise).
- There is impressed transformer primary current and/or dynamic limitation of the input current (e.g., for saturation of the magnetic circuit of the transformer due to control unsymmetries); furthermore, thereby, current spikes on the primary resulting from reverse-recovery currents of the output diodes for buck-derived converter systems are avoided. Also, a conduction overlap of the power transistors, i.e., switching state $s_- = s_+ = 1$ and/or $s_R = s_S = s_T = 1$ becomes admissible and does not lead to a short circuit of the line-to-line voltage.
- The maximum volt seconds resulting across the transformer are limited and are defined by the pulse period and the output voltage (and not by the mains voltage as for buck-derived converter systems); therefore, also for heavily varying mains voltage, a good transformer utilization can be obtained (for approximately constant output voltage).
- The blocking voltage of the output diodes is defined by the output voltage (with low inductance) and is independent of the mains voltage. This is of special advantage for wide input voltage range and constant output voltage and/or, in general, for high output voltages. (For buck-type converters, the blocking voltage stress on the output diodes is defined by the mains voltage. Due to the transformer stray inductance and due to the output inductance, one has no voltage level for a direct limitation of the blocking voltage; this is in analogy to the limitation of the voltages on the primary for boost-derived converter systems, see Section VI-C).
- There is good cross regulation for more than one output voltage under the assumption of close coupling of the secondary windings (see [38, p. 1]) because no filter inductances are in series with the different output voltages. (A similar system behavior can be obtained for buck-type converters only for magnetic coupling of the output inductances. This involves a relatively high realization effort, however.)

The disadvantages are as follows.

- There is discontinuous output current shape and/or a relatively high current stress on the output capacitors and on the output diodes.
- There is a right-half-plane zero of the transfer function between modulation depth of the converter (according to the duty ratio for dc-to-dc converters) and the average output current.
- A limitation of the transformer primary voltage and/or of the blocking voltage across the power semiconductors on the primary is required because, otherwise, the transformer stray inductance would lead to high overvoltages for a change of the converter switching state and/or a step change of the transformer primary current.
- There is an unfavorable transformer dimensioning for a wide variation range of the input and output voltages, because the transformation ratio (N_1/N_2) has to be selected such that, for minimum output voltage, a primary voltage can still be generated which balances the maximum input voltage.
- In general, no direct startup and no direct current limitation for an output voltage short circuit is possible, which is a more complex startup than for buck-derived converter systems; the basic reason is that the system function is dependent on a minimum value of the output voltage (which, in turn, is dependent on the input voltage).

As becomes clear by the list given, the converter system proposed has a number of advantages which motivate a closer investigation, which is beyond the basic considerations of this paper. Here, in particular, the soft-switching operation and the possibility of operating the system with low pulse rate (as proposed in [39]–[41] for the conventional VIENNA Rectifier) shall be investigated. Furthermore, the establishment of guidelines for converter dimensioning and a more detailed experimental analysis are planned.

Concluding, one has to point out that based on the basic structure of the system proposed and investigated in this paper, a new single-stage buck-type converter system with *impressed output current* and *impressed input voltage* can be formed (VIENNA Rectifier III, [42]) by dual exchange of the input-side and output-side energy storage devices. According to first investigations, this new system also has high power density and high efficiency. Therefore, the aim of further research also will be a comprehensive and comparative analysis of single-stage and two-stage (e.g., VIENNA Rectifier I [29] with dc-to-dc converter connected in series [43]) three-phase PWM rectifier systems regarding realization cost, efficiency, and volume. The results also will determine the future trends of the research at the Technical University Vienna in the area of three-phase rectifier systems with low effects on the mains.

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