Novel Single-Stage Isolated Natural Ohmic Mains Behaviour Fixed Voltage Transfer Ratio Three-Phase Rectifier Using Monolithic Bidirectional 600 V GaN Transistors

S. Weihe, D. Menzi, J. Huber, and J. W. Kolar
Power Electronic Systems Laboratory, ETH Zurich, Switzerland
weihe@lem.ee.ethz.ch

***Abstract*—This paper introduces a novel phase-modular single-stage isolated three-phase PFC rectifier with a fixed (load-independent) ratio between grid voltage amplitude and dc output voltage. The ac front-end employs star-connected half-bridges with recently developed 600-V GaN monolithic bidirectional switches (M-BDSs) to directly connect to a 400-V (line-to-line rms) three-phase mains. Series-resonant compensation of the transformer's leakage inductance and operation of the system at the resonance frequency results in a load-independent dc output voltage, directly defined by the grid voltage amplitude, and natural ohmic mains behaviour, i.e., sinusoidal input currents, without any closed-loop control. Accordingly, the converter features low complexity in both, the circuit structure and the modulation, and thus enables high reliability / availability and low assembly effort. The paper provides a detailed analysis of the converter system operating principle, determines the main power component stresses, and validates the concept by circuit simulations.**

***Index Terms*—three-phase ac-dc converter, PFC rectifier, high-frequency isolation, fixed-voltage transfer ratio, single-stage power conversion, monolithic bidirectional GaN transistors, M-BDS.**

I. Introduction

Typically, isolated three-phase power-factor-correction (PFC) rectifiers for applications like telecom power supplies, welding current sources, or induction heaters are realized as two-stage systems featuring a (non-isolated) ac-dc PFC rectifier front-end ensuring ohmic mains behaviour with sinusoidal grid currents and a subsequent dc-dc converter providing galvanic isolation with a high-frequency (HF) transformer [1]. Utilizing the transformer's stray inductance for the circuit functionality, the isolated dc-dc converter can be realised, for example, as a dual-active-bridge (DAB) converter or as an LLC/series-resonant converter (SRC). If operated at the resonance frequency, a fixed input-output voltage ratio results for the SRC, i.e., it behaves like a "dc transformer" (DCX) [2]. As an alternative to combining an integrated non-isolated three-phase ac-dc PFC stage with a DCX converter, multi-port DCX converters can be combined with three front-end single-phase PFC ac-dc stages, thus realizing a phase-modular three-phase mains interface [3, 4]. Such two-stage approaches, however, come with high component count and realization effort, and processing the power twice ultimately limits the conversion efficiency.

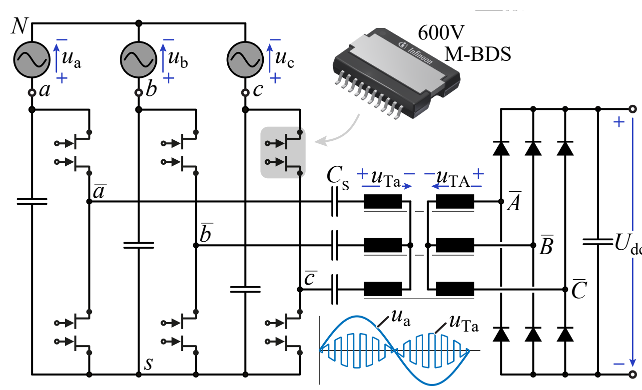

Fig. 1. Power circuit of the iYR$_x$ with a star-(Y)-connected primary-side transformer configuration which employs 600 V GaN M-BDSs in the ac front-end to directly interface with the 325 V_{peak} (line-to-neutral; 400 V line-to-line rms) three-phase grid.

Therefore, *single-stage* isolated three-phase PFC ac-dc converters [5–24] have been a focus of research in the past decade. Advantageously, modern 600 V GaN monolithic BDSs (M-BDSs) [25] allow to extend the functionality of three-phase dc-dc DCX converters [26] to also accept three-phase ac input voltages [23, 24] as presented in **Fig. 1**. There, the required M-BDS blocking voltage is defined by the line-to-neutral voltage amplitude of $\hat{U}_{ac} = 325\,\mathrm{V}$ in a 400 V (line-to-line rms) mains and thus 600-V-rated M-BDSs have sufficient blocking-voltage margin[1] [23, 24]. However, most of these single-stage concepts require relatively complicated control and/or modulation strategies to provide advanced functionality like buck-boost output voltage regulation, which, alas, comes at the price of potentially reduced robustness and reliability; i.e., concepts with reduced functionality and thus lower control complexity like [21, 27] might be beneficial for certain applications that, e.g., do not require a tightly controlled dc output voltage.

Therefore, this paper proposes the novel single-stage isolated three-phase PFC rectifier depicted in **Fig. 1** (and the functionally

[1]Typically, the power transistors are subject to the line-to-line voltage amplitude $\sqrt{3}\hat{U}_{ac} = 565\,\mathrm{V}$ and thus a blocking voltage of 900 V is required.

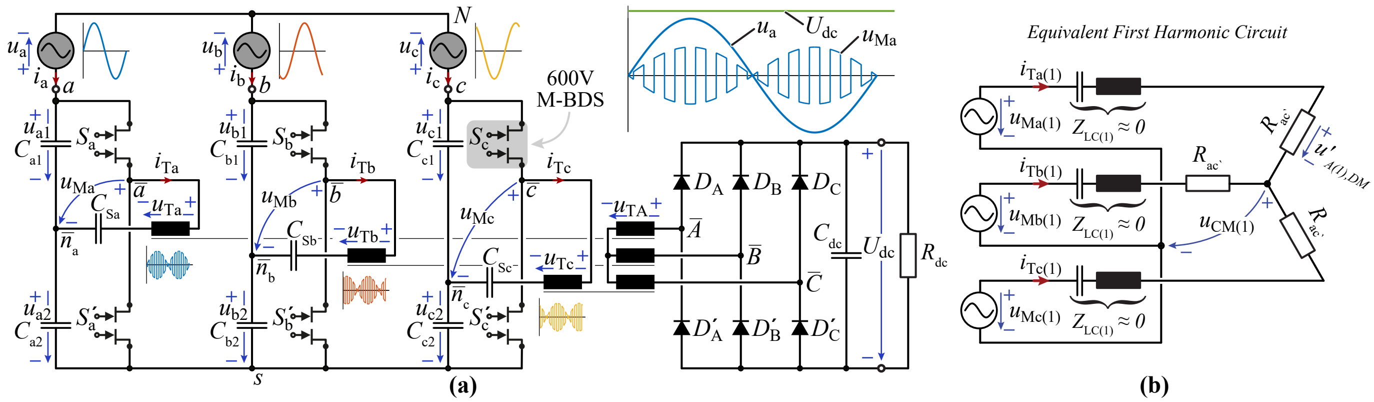

Fig. 2. **(a)** Alternative, i.e. functionally equivalent, realization of the iYR$_x$ topology of **Fig 1** with a split ac-link primary side transformer configuration. The 600 V M-BDSs employed in the ac front-end generate grid-voltage amplitude-modulated square-wave voltages u_{Ma}, u_{Mb}, u_{Mc} applied to the resonant tanks, which are 120° HF phase shifted (indicated for phase a with a low switching frequency for better visibility). The capacitors $C_{\mathrm{Sa}}, C_{\mathrm{Sb}}, C_{\mathrm{Sc}}$ are connected in series with the transformer (with turns ratio $N_1 : N_2$) to compensate the corresponding phase leakage inductances L_{S}, i.e., to form resonant tanks tuned to the switching frequency f_{sw}. The secondary-side converter stage is realized solely with diodes, i.e., passive rectification, but can also be realized by self-driven synchronous rectification with conventional transistors (unipolar voltage blocking capability). **(b)** Simplified primary-side-related equivalent circuit considering only the first switching-frequency harmonic voltage component of the square-wave voltages generated by the power semiconductor devices.

equivalent realization in **Fig. 2a**) with low complexity in both, the circuit structure and the modulation, which, accordingly, results in low assembly effort and high reliability/availability: Star-(Y)-connected half-bridges with recently developed 600-V GaN M-BDSs are employed in the ac front-end which directly connects to the 400 V three-phase mains. In each phase a resonant tank is formed by the series capacitor C_{s} and the leakage inductance L_{s} of the HF transformer and the secondary-side converter stage is realized as a simple B6 diode rectifier. Operating the front-end half-bridges with a constant 50% duty cycle at the resonance frequency ($f_{\mathrm{s}} = f_0 \approx 1/(2\pi\sqrt{C_{\mathrm{s}}L_{\mathrm{s}}})$), advantageously, sinusoidal grid currents (with unity power factor) are naturally established.[2] No closed-loop control or complex space-vector modulation is required and a fixed, (almost) load-independent ratio between the grid voltage amplitude and the dc output voltage results. The topology is thus referred to as an isolated Y-rectifier with a DCX-like operation, or iYR$_x$.

In the following, first **Section II** derives the operating principle of the iYR$_x$ based on a first-harmonic approximation (FHA), which then **Section III** also uses for providing design guidelines, analytic expressions for key component stresses, and a design example for the specifications in **Tab. I**. Finally, **Section IV** employs detailed circuit simulations to verify both, the operating principle and the accuracy of the FHA-based modelling and design. **Section V** concludes the paper.

II. Operating Principle

The aim of this section is, first, to derive the fundamental voltage and current formation in the HF transformer, and second, to derive an analytic expression for the power transfer. This analysis is performed here considering the alternative iYR$_x$ power circuit structure depicted in **Fig. 2a** which features an HF

[2]As detailed below, this is conceptually based on [28]; there, however, PWM is employed to synthesize sinusoidal primary-side HF transformer voltages, i.e., the switching frequency is higher than the transformer operating frequency.

Table I
System Specifications.

Description	Identifier	Value	Unit
Grid phase voltage[1]	U_{ac}	230	$\mathrm{V_{RMS}}$
Grid current	I_{ac}	9.6	$\mathrm{A_{RMS}}$
Grid frequency	f_{ac}	50	Hz
Switching frequency	f_{sw}	72	kHz
dc power	P_{dc}	6.6	kW
dc voltage	U_{dc}	400	V
dc current	I_{dc}	16.5	A

[1]line-to-neutral voltage

transformer primary-side open-winding-realization (with turns ratio $N_1 : N_2$ and a leakage inductance L_{S}) which connect to the split input filter capacitors (e.g., $C_{\mathrm{a1}}, C_{\mathrm{a2}}$ in phase a). Note that similar derivation steps can also be applied to the iYR$_x$ in **Fig. 1** (which, however, shows a more complicated resonant tank voltage formation) resulting in an identical transformer current formation and component stresses as determined in **Section III**.

A. Resonant Tank Voltage and Current Formation

The symmetric three-phase grid voltages u_{x} ($x \in a, b, c$) are defined as

$$u_{\mathrm{x}} = \hat{U}_{\mathrm{ac}} \sin(2\pi f_{\mathrm{ac}} t + \phi_{\mathrm{x}}) \quad \phi_{\mathrm{x}} \in \{0, -2\pi/3, 2\pi/3\}, \quad (1)$$

with the line-to-neutral (phase) voltage amplitude $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V}$ and the frequency $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$. Three 120° phase-shifted PWM switching signals S_{x} with 50% on-time are applied to each M-BDS half-bridge as

$$S_{\mathrm{x}} = 0.5\,\mathrm{sgn}(\sin(2\pi f_{\mathrm{sw}} t + \phi_{\mathrm{x}})) + 0.5. \quad (2)$$

Thus, three 120° phase-shifted square wave voltages u_{Ma}, u_{Mb}, u_{Mc} amplitude-modulated by the respective grid voltage, are generated. E.g., for phase a the resonant-tank voltage is defined as

$$u_{\mathrm{Ma}} = \frac{\hat{U}_{\mathrm{ac}}}{2} \sin\left(2\pi f_{\mathrm{ac}} t\right) \operatorname{sgn}\left(\sin\left(2\pi f_{\mathrm{sw}} t\right)\right), \tag{3}$$

and toggles between $\pm\frac{1}{2}u_{\mathrm{a}}(t)$ as highlighted in **Fig. 2a** and **Fig. 3a** (dashed blue line).

In each phase, a series capacitor C_{S} compensates the HF transformer stray inductance L_{S} at the switching frequency f_{sw} (i.e., $f_{\mathrm{sw}} = f_0 \approx \frac{1}{2\pi\sqrt{L_{\mathrm{S}} C_{\mathrm{S}}}}$). This results in a resonant operating mode similar to a DCX dc-dc converter, with zero the resonant tank impedance $Z_{\mathrm{LC}}(f_0) \approx 0$ at the FH resonant-tank voltage component $u_{\mathrm{Ma(1)}}$. In contrast, for higher-order harmonics, Z_{LC} acts as a large impedance and large attenuation is provided at, e.g., $3f_0$ and $5f_0$ as highlighted in **Fig. 4**. Note that large transformer leakage inductance values L_{S} increase the attenuation of higher-order harmonics.

Accordingly, the converter behaviour can be assessed with an FHA [29] based on the simplified circuit shown in **Fig. 2b**. and the FH resonant-tank voltage $u_{\mathrm{Ma(1)}}$ of phase a can be defined as

$$u_{\mathrm{Ma(1)}} = \frac{\hat{U}_{\mathrm{ac}}}{2} \sin\left(2\pi f_{\mathrm{ac}} t\right) \frac{4}{\pi} \sin\left(2\pi f_{\mathrm{sw}} t\right). \tag{4}$$

Note that the amplitude-modulated FH voltages $u_{\mathrm{Ma(1)}}$, $u_{\mathrm{Mb(1)}}$, $u_{\mathrm{Mc(1)}}$ applied to the resonant tank in **Fig. 3a** comprise a common-mode (CM) component $u_{\mathrm{CM(1)}} = \frac{1}{3}\sum_{x\in a,b,c} u_{\mathrm{Mx(1)}}$ equal to

$$u_{\mathrm{CM(1)}} = \frac{\hat{U}_{\mathrm{ac}}}{\pi} \cos\left(2\pi\left(f_{\mathrm{sw}} - f_{\mathrm{ac}}\right)t\right), \tag{5}$$

with a frequency $f_{\mathrm{CM(1)}} = f_{\mathrm{sw}} - f_{\mathrm{ac}}$, which cannot drive any current in the open star point secondary-side transformer windings. Thus, similar to [28], only the differential-mode (DM) FH voltage components are relevant for the formation of the resonant tank currents and for the HF power transfer. E.g., for phase a the DM FH voltage $u_{\mathrm{Ma(1),DM}} = u_{\mathrm{Ma(1)}} - u_{\mathrm{CM(1)}}$ is equal to

$$u_{\mathrm{Ma(1),DM}} = -\frac{\hat{U}_{\mathrm{ac}}}{\pi} \cos\left(2\pi\left(f_{\mathrm{sw}} + f_{\mathrm{ac}}\right)t\right), \tag{6}$$

with a frequency $f_{\mathrm{sw}} + f_{\mathrm{ac}}$ and a constant amplitude of $\frac{\hat{U}_{\mathrm{ac}}}{\pi}$ as depicted in **Fig. 3b**. Thus, resonance-tank currents $i_{\mathrm{Ta(1)}}, i_{\mathrm{Tb(1)}}, i_{\mathrm{Tc(1)}}$ (**Fig. 3c**) occur at the same frequency $f_{\mathrm{sw}} + f_{\mathrm{ac}}$. It's worth highlighting that in contrast to [28] the secondary-side passive rectification stage is current-driven (instead of voltage driven): The HF transformer leakage inductances L_{s} force three diodes to conduct at any point in

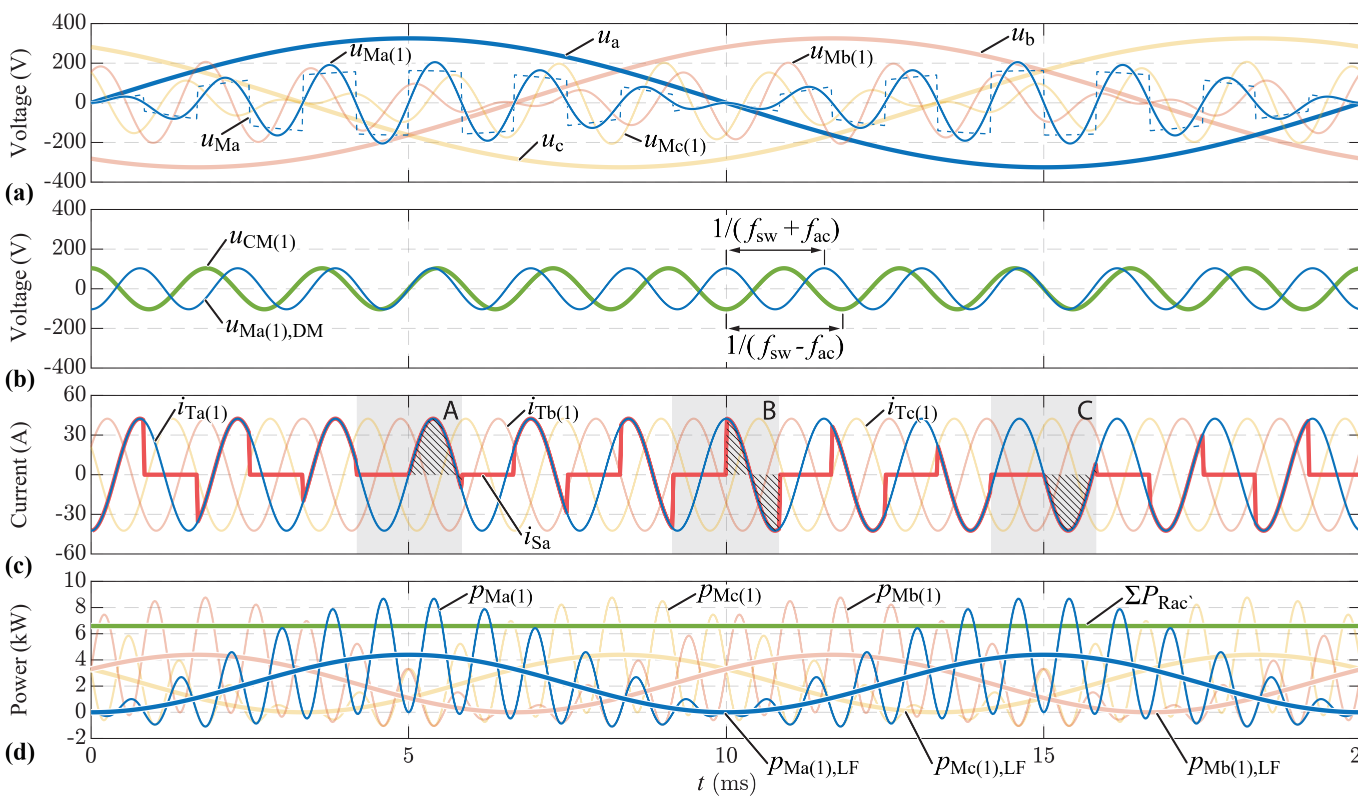

Fig. 3. Graphical illustration of the first-harmonic approximation (FHA) of the three-phase resonant circuit voltages and currents formed by the converter in **Fig. 2** for a passive secondary-side converter stage realization with diodes: The square-wave ac front-end switch-node voltage u_{Ma} can be substituted with its first harmonic $u_{\mathrm{Ma(1)}}$ to explain the natural unity power factor operation of the iYR$_{\mathrm{x}}$. Note that the driving voltages $u_{\mathrm{Ma(1)}}$, $u_{\mathrm{Mb(1)}}$, $u_{\mathrm{Mc(1)}}$ do not sum to zero and thus a common-mode (CM) voltage $u_{\mathrm{CM(1)}}$ with $f_{\mathrm{CM(1)}} = f_{\mathrm{sw}} - f_{\mathrm{ac}}$ results. Analysing phase a, the differential voltage generated drives a transformer current $i_{\mathrm{Ta(1)}}$ with a frequency of $f_{\mathrm{sw}} + f_{\mathrm{ac}}$. The multiplication of $u_{\mathrm{Ma(1)}}$ and $i_{\mathrm{Ta(1)}}$ results in the instantaneous power delivery $p_{\mathrm{Ma(1)}}$ whose low-frequency component $\bar{p}_{\mathrm{Ma(1)}}$ corresponds to the $\sin^2(2\pi f_{\mathrm{ac}} t)$ per-phase power delivery associated with unity power factor operation.

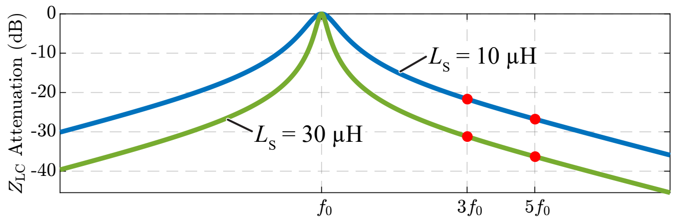

Fig. 4. Attenuation of higher harmonics by the resonant tank impedance Z_{LC}, with attenuation improving for larger values of transformer leakage inductance L_{S}.

time[3] and in each phase the high- and low-side diode have 50% conduction time during a $f_{\mathrm{sw}}+f_{\mathrm{ac}}$ period. Thus, the secondary-side converter stage effectively mimics a resistive behaviour at the FH. Therefore the three-phase diode rectifier can be represented by an equivalent primary-side-related resistive three-phase load R'_{ac} as highlighted in **Fig. 2b** and the resonant tank current of, e.g., phase a is defined by

$$i_{\mathrm{Ta}(1)} = -\hat{i}_{\mathrm{Ta}(1)} \cos\left(2\pi\left(f_{\mathrm{sw}}+f_{\mathrm{ac}}\right)t\right), \tag{7}$$

with $\hat{i}_{\mathrm{Ta}(1)} = \frac{\hat{U}_{\mathrm{ac}}}{R_{\mathrm{ac}}'\pi}$ as shown in **Fig. 3c**. The equivalent resistance can be calculated as

$$R_{\mathrm{ac}}' = \left(\frac{N_1}{N_2}\right)^2 \frac{2\pi+3\sqrt{3}}{6\pi} R_{\mathrm{dc}}. \tag{8}$$

Note that the rectifier stage voltages are directly defined by the diode conduction states and, e.g., for phase a the FH DM component results to

$$u_{\mathrm{A}(1),\mathrm{DM}} = \frac{U_{\mathrm{dc}}}{2}\frac{4}{\pi}\cos\left(2\pi\left(f_{\mathrm{sw}}+f_{\mathrm{ac}}\right)t\right). \tag{9}$$

With the FH resonant tank impedance approximately equal to zero, the FH DM voltage components of the primary- and secondary-side stage in each phase need to cancel out, e.g., $u_{\mathrm{Ma}(1),\mathrm{DM}} \approx u'_{\mathrm{A}(1),\mathrm{DM}} = \frac{N_1}{N_2}u_{\mathrm{A}(1),\mathrm{DM}}$. Thus, for a given transformer turns ratio $\frac{N_2}{N_1}$, the dc output voltage is directly linked to the grid line-to-neutral voltage amplitude[4], defining a natural input-output voltage ratio as

$$\frac{U_{\mathrm{dc}}}{2}\frac{4}{\pi}\frac{N_1}{N_2} \approx \frac{\hat{U}_{\mathrm{ac}}}{\pi} \rightarrow U_{\mathrm{dc}} \approx \frac{\hat{U}_{\mathrm{ac}}}{2}\frac{N_2}{N_1}. \tag{10}$$

B. HF Power Transfer Characteristics

To simplify the calculations, the peak primary-side phase a transformer current $\hat{i}_{\mathrm{Ta}(1)}$ in (7) can be defined alternatively by assuming an ideally lossless three-phase HF power transfer $P_{\mathrm{dc}} = \frac{3}{2}\hat{u}_{\mathrm{Ma}(1),\mathrm{DM}}\,\hat{i}_{\mathrm{Ta}(1)}$. The resulting instantaneous FH power in phase a,

$$p_{\mathrm{Ma}(1)} = u_{\mathrm{Ma}(1)} \cdot i_{\mathrm{Ta}(1)} = \underbrace{\frac{2}{3}P_{\mathrm{dc}}\sin\left(2\pi f_{\mathrm{ac}}t\right)^2}_{p_{\mathrm{Ma}(1),\mathrm{LF}}} + \underbrace{\frac{P_{\mathrm{dc}}}{3}\left(\cos\left(4\pi\left(f_{\mathrm{sw}}+f_{\mathrm{ac}}\right)t\right) - \cos\left(4\pi f_{\mathrm{sw}}t\right)\right)}_{p_{\mathrm{Ma}(1),\mathrm{HF}}} \tag{11}$$

is presented in **Fig. 3d**. Note that its low-frequency (LF) component $p_{\mathrm{Ma}(1),\mathrm{LF}}$ corresponds to the natural $\sin^2(2\pi f_{\mathrm{ac}}t)$ power delivery associated with unity power factor sinusoidal grid currents in each phase. In contrast, the HF power component $p_{\mathrm{Ma}(1),\mathrm{HF}}$ represents an HF power fluctuation which needs to be filtered by the input/grid filter along with the higher order harmonic components.

Note that the sinusoidal grid current formation can also be derived by investigating the high-side M-BDS S_{a} current i_{Sa} (with a switching-frequency average value approximately equal to the phase a grid current, i.e., $\bar{i}_{\mathrm{Sa}} \approx i_{\mathrm{a}}$) highlighted in **Fig. 3c**: Due to the elevated frequency of the transformer FH current $i_{\mathrm{Ta}(1)}$ (at $f_{\mathrm{sw}}+f_{\mathrm{ac}}$) compared to the switching frequency f_{sw} of S_{a}, the rectified current shows a grid frequency f_{ac} time varying value $\bar{i}_{\mathrm{Sa}}$. Three distinct switching periods are highlighted at peak positive grid voltage (A; $\bar{i}_{\mathrm{Sa}} \approx \hat{I}_{\mathrm{ac}}$), grid zero voltage (B; $\bar{i}_{\mathrm{Sa}} \approx 0$) and peak negative grid voltage (C; $\bar{i}_{\mathrm{Sa}} \approx -\hat{I}_{\mathrm{ac}}$).

III. Design and Component Stresses

To verify the concept of the $\mathrm{iYR_x}$ a basic design example is conducted for a 6.6 kW converter which conforms to the system specifications outlined in **Tab. I**. Further, a leakage inductance $L_{\mathrm{s}} = 10\,\mu\mathrm{H}$ is considered, as such values can be easily realized in the transformer design without the need for explicit series inductors.

A. Component Value Selection

Aiming at operation in a $U_{\mathrm{ac}} = 230\,\mathrm{V_{rms}}$ grid and an output voltage of $U_{\mathrm{dc}} = 400\,\mathrm{V}$, a suitable transformer turns ratio $N_1 : N_2 = 2:5$ is selected according to (10).

The goal of the series capacitors C_{s} in **Fig. 2a** is to assure a resonant frequency $f_0 = f_{\mathrm{sw}}$. Note that the split input capacitors $C_{\mathrm{x1}}, C_{\mathrm{x2}}$ (With equal capacitance values) also slightly impact the resonance frequency as

$$C_{\mathrm{S}} = \frac{C_{\mathrm{x1}}}{4\pi^2 f_{\mathrm{sw}}^2 L_{\mathrm{S}} C_{\mathrm{x1}} - \frac{1}{2}} \approx \frac{1}{4\pi^2 f_{\mathrm{sw}}^2 L_{\mathrm{S}}}. \tag{12}$$

Here, the input capacitors are selected based on a 2% reactive input current limit at nominal power operation to $C_{\mathrm{x1}} = C_{\mathrm{x2}} = 5\,\mu\mathrm{F}$ and thus the series capacitance results to $C_{\mathrm{S}} = 514\,\mathrm{nF}$. Note that 50% duty cycle applied in the ac front-end bridge-legs results in zero LF voltage excitation of C_{S}[5]. Thus its (HF)

[3] This is different to the standard six-pulse diode rectifier where only the two diodes connected to the instantaneously largest line-to-line voltage conduct a current.

[4] Similar to a DCX converter, any FH voltage difference leads to an increase in the resonant tank current level and thus to a higher power transfer until the natural input-output voltage ration is established [30, 31].

[5] Note that the series capacitance C_{S} in **Fig. 1** must additionally block LF voltages of up to 50% $\hat{U}_{\mathrm{ac}}$.

peak voltage $\hat{u}_{C_S}$ can be easily estimated given the peak energy storage of the leakage inductance L_S,

$$\hat{u}_{C_S} = \sqrt{\frac{L_S}{C_S}} \hat{i}_{Ta(1)}, \tag{13}$$

and with $\hat{i}_{Ta(1)} = 42.5\,A$ results to $\hat{u}_{C_S} = 187\,V$. Note that a load step (as highlighted in **Section IV**) is associated with transient resonant tank over-voltage and -current. These can be quantified using the methods in [32], thus allowing for appropriate safety margins.

The dc-link capacitor FH rms current stresses can be analytically derived as

$$i_{C_{dc}(1),rms} = \hat{i}_{Ta(1)} \frac{N_1}{N_2} \sqrt{\frac{3}{\pi}\left(\frac{\sqrt{3}}{4} - \frac{3}{\pi} + \frac{\pi}{6}\right)}. \tag{14}$$

Note that this current occurs at a frequency $6 f_{sw}$ and thus an HF pk-pk dc-link voltage ripple ΔV criterion can be directly translated into a suitable capacitance value

$$C_{dc} = \frac{\Delta Q}{\Delta V} = \frac{\frac{\sqrt{2}\, i_{C_{dc}(1),rms}}{\pi\, 6 f_{sw}}}{\Delta V}. \tag{15}$$

E.g., a value of $\Delta V = 0.5\,V$ corresponds to a low output capacitance value of only $C_{dc} = 1.42\,\mu F$. Note that, aiming at providing a certain bulk energy storage in case of a load step [32], $C_{dc} = 40\,\mu F$ is considered in **Tab. II**, which, however, does not impact the steady-state simulation waveforms in **Sec. IV**.

B. Component Stresses and Loss Modelling

The relevant iYR$_x$ (**Fig. 2a**) power component current stresses in **Tab. III** are derived analytically from the FH peak transformer current $\hat{i}_{Ta(1)}$ and can be utilized to estimate the losses of the primary components. Using the magnitude of diode current stresses based on the FHA the IDH20G65C6 650 V SiC diode is selected as an appropriate device for the secondary side rectification. The parameters V_{th} and R_{diff} (as a function of junction temperature T_j; a typical $R_{th,JC} = 0.8\,K/W$ of the datasheet is considered) can be utilized to evaluate the diode losses using the equation in **Tab. III**[6]. The M-BDS are blocking voltages of up to $\hat{U}_{ac} = 325\,V$, and the switching and conduction losses are estimated by considering fractional parallel scaling N_f of the 1st Gen 600 V / 140 mΩ device presented in [25]. It should be noted that this is a conservative estimation, as the continuous development of next-gen M-BDSs is expected to result in substantial performance improvements. The analytically derived M-BDS turn-on/-off currents are highlighted with red and green curves, respectively, in **Fig. 7**[7]. Multiple parallel chips in a PG-DSO package are assumed, and considering both, the switching and the junction temperature dependent conduction losses[6], $N_f = 7$ (maximum $R_{DSon} = 20\,m\Omega$) is selected to assure a maximum junction temperature $T_j \leq 100\,°C$.

Last, the losses in the filter and series capacitors are neglected (assuming a high-quality dielectric a low dissipation factor results) and aiming at simple engineering design guidelines, the HF transformer losses (P_{Ta}) are calculated assuming a typical efficiency $\eta_T = 99.5\%$ (**Tab. III**).

IV. Steady-State and Transient Simulation Results

Fig. 5 presents the proof-of-concept iYR$_x$ waveforms obtained in PLECS [34] for $U_{ac} = 230\,V_{rms}$ and for the power component values listed in **Tab. II** where naturally sinusoidal grid currents without the need for close-loop control can be observed. A load step from 3.3 kW to 6.6 kW at $t = 20\,ms$ (R_{dc} is reduced from 33 Ω to 16.5 Ω) verifies the largely load-independent output voltage U_{dc} of the iYR$_x$. Note that a grid-side EMI filter needs to be introduced in a practical converter realization to confine the switching-frequency noise of the unfiltered currents i_a, i_b, i_c. **Fig. 5** shows the converter waveforms during two switching periods around $t = 30\,ms$: The primary-side-related secondary-side transformer voltages u'_{TA}, u'_{TB}, u'_{TC} and the corresponding resonant tank currents i_{Ta}, i_{Tb}, i_{Tc} indicate a local average of the transformer power flow that is proportional to the magnitude of the corresponding grid voltage. The grid voltage to output voltage correlation described by **(10)** is further validated in **Fig. 6** through nominal power simulation with ±10% grid voltage amplitude steps applied, where a proportional change in U_{dc} is observed.

A. Loss Analysis Results

The resulting system stresses and losses based on the FHA are compared with the simulation results in **Tab. III**. The overall system losses (considering that the major loss sources, i.e., the diodes, transformers and M-BDSs) are estimated to be in the region of 180 W (corresponding to an overall system efficiency of $\eta \approx 97\%$), and a close matching between the analytic (FHA) and simulation results can be observed. The main source of deviations is the fact that the HF transformer

[6] A thermal interface material (TIM) with a thermal impedance of $52\,K\,mm^2/W$ [33] is considered to interface the device case and the heat sink with a (maximum) temperature of 80 °C.

[7] For the three highlighted switching periods (A,B,C) in **Fig. 3c** the following switched currents occur in the phase a: At peak grid voltage u_a (A,C) turn on and turn off occur at the zero crossing of the transformer current $i_{Ta(1)}$; In contrast, at the grid zero crossing (B) turn on and turn off occur at the maxima and minima of the transformer current, respectively. I.e., the switched currents are formed by the envelope of the beat frequency of the transformer current $i_{Ta(1)}$ and the FH of the switching signal S_a, and the FHA allows to predict both, the switched voltages and currents, which can be used to evaluate the hard-switching energy and losses over the grid period analytically as shown in **Tab. III**.

Table II
Selected Converter Parameters.

Description	Identifier	Value	Unit
Input capacitance	C_{x1}, C_{x2}	5	µF
M-BDS	S_a	20	mΩ
Series capacitance	C_S	514	nF
Leakage inductance	L_S	10	µH
Turns ratio	$N_1 : N_2$	2 : 5	
Diodes	D_A	650 V SiC (IDH20G65C6)	
dc capacitance	C_{dc}	40	µF

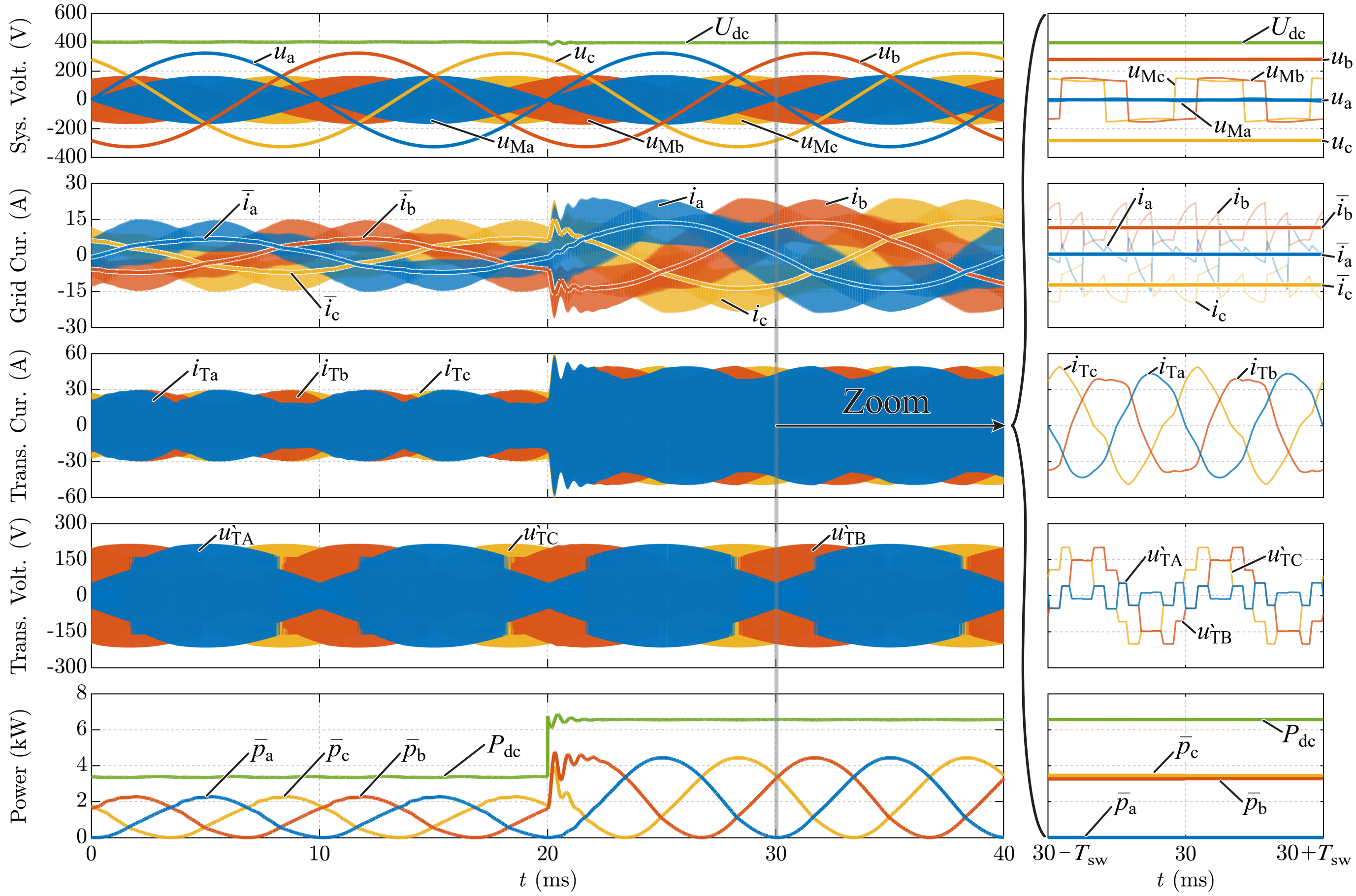

Fig. 5. Circuit simulation results of the iYR$_x$ topology in **Fig. 2** with diodes utilized for the secondary-side converter stage ($U_{ac} = 230\,\mathrm{V\,rms}$, $f_0 = f_{sw} = 72\,\mathrm{kHz}$ and $N_1 : N_2 = 2 : 5$) validating its natural unity power factor operation. A load step from $3.3\,\mathrm{kW}$ to $6.6\,\mathrm{kW}$ at $t = 20\,\mathrm{ms}$ highlights the largely load-independent output voltage $U_{dc} \approx 400\,\mathrm{V}$ of the iYR$_x$.

currents in **Fig 5** (zoom in) are not fully sinusoidal as assumed by the FHA. **Fig. 7** compares the analytic FHA and simulated M-BDS turn on/off currents. Note that increasing the leakage inductance L_S from $10\,\mu\mathrm{H}$ to $30\,\mu\mathrm{H}$ results in an improved attenuation of the higher-harmonic components, and thus to a more close matching of the FHA and the simulation results.

V. Conclusion

Low-complexity and robust unidirectional isolated three-phase ac-dc converters with unity power factor operation are of paramount importance for many applications. The emergence of 600 V GaN monolithic bidirectional switches (M-BDSs) enables new converter topologies with low component count and complexity and this paper introduces the novel isolated Y-rectifier with a DCX-type operation (iYR$_x$), which enables single-stage three-phase PFC rectification with a galvanically isolated and constant dc output voltage. Advantageously, there is no need for any kind of closed-loop control as explained by the mathematical derivation (based on a first-harmonic (FH) approximation) revealing the natural unity power factor and DCX-type operating principle of the iYR$_x$. Additionally, the theoretical operation is validated with simulations of load and grid voltage steps, highlighting the predictable/reliable load-independent input-output voltage relation. Lastly, the stresses of the main power components for a 6.6 kW virtual prototype are discussed. Design guidelines based on an analytic FH derivation are provided and match closely the simulated performance.

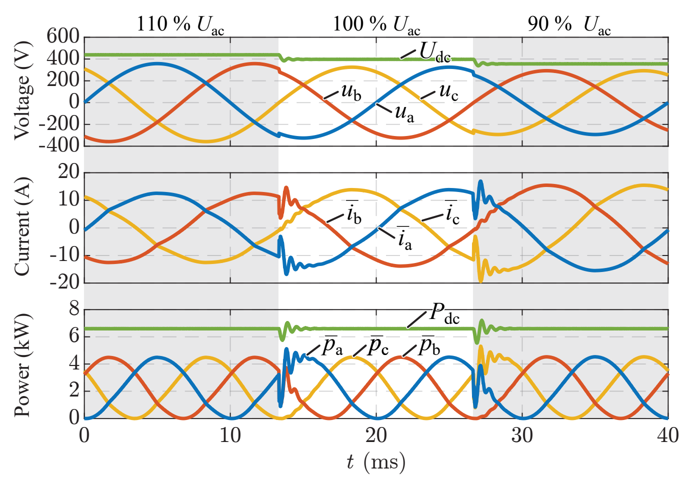

Fig. 6. Output voltage to grid dependency highlighted by simulation of the iYR$_x$ with a constant power draw of 6.6 kW. As can be observed, a grid voltage change of $\pm 10\%$ directly correlates to an equal $\pm 10\%$ change in output voltage U_{dc} according to the voltage dependency discussed in **Section II**.

TABLE III
COMPONENT STRESSES AND LOSS EVALUATION FOR THE CONVERTER IN FIG. 2.

Parameter	Analytical Solution	Analytical Result	Simulation Result	Unit	Error
U_{dc}	$\frac{\hat{U}_{\mathrm{ac}}}{2}\frac{N_2}{N_1}$	407	396	V	2.56%
$\hat{i}_{\mathrm{Ta}}$	$\frac{P_{\mathrm{dc}}}{3}\frac{2\pi}{\hat{U}_{\mathrm{ac}}}$	42.5	50.6	A	−16.0%
I_{Ta}	$\hat{i}_{\mathrm{Ta}}/\sqrt{2}$	30.1	31.1	$\mathrm{A_{RMS}}$	−3.49%
$I_{\mathrm{Sa}} = I_{\mathrm{Sa'}}$	$\hat{i}_{\mathrm{Ta}}/2$	21.2	22.0	$\mathrm{A_{RMS}}$	−3.45%
$I_{\mathrm{DA}} = I_{\mathrm{DA'}}$	$\frac{N_1}{N_2}\frac{\hat{i}_{\mathrm{Ta}}}{2}$	8.5	8.8	$\mathrm{A_{RMS}}$	−3.49%
$I_{\mathrm{DA_{avg}}}$	$\frac{N_1}{N_2}\frac{\hat{i}_{\mathrm{Ta}}}{\pi}$	5.4	5.5	A	−2.46%
$P_{\mathrm{Sa,Cond}}$	$R_{\mathrm{SS(on)}}(T_{\mathrm{jM}})\ I_{\mathrm{Sa}}^2/N_{\mathrm{f}}$	12.7	13.7	W	−6.84%
$P_{\mathrm{Sa,Sw}}$	$\frac{N_{\mathrm{f}} f_{\mathrm{sw}}}{\pi}\left(\frac{(k_{2,\mathrm{s}}+k_{2,\mathrm{h}})\pi\hat{U}_{\mathrm{ac}}^2}{4}+\frac{(k_{1,\mathrm{s}}+k_{1,\mathrm{h}})\hat{i}_{\mathrm{Ta}}\hat{U}_{\mathrm{ac}}}{2N_{\mathrm{f}}}\right)$	5.2	4.1	W	25.3%
P_{Ta}	$(1-\eta_{\mathrm{T}})\ P_{\mathrm{dc}}/3$	11.0	11.4	W	−3.44%
P_{DA}	$V_{\mathrm{TH}}(T_{\mathrm{jD}})\ I_{\mathrm{DA_{avg}}} + R_{\mathrm{DIFF}}(T_{\mathrm{jD}})\ I_{\mathrm{DA}}^2$	6.0	6.3	W	−4.83%
P_{Total}	$6(P_{\mathrm{Sa,Cond}}+P_{\mathrm{Sa,Sw}})+3P_{\mathrm{Ta}}+6P_{\mathrm{DA}}$	177	179	W	−1.33%
η	$P_{\mathrm{dc}}/(P_{\mathrm{dc}}+P_{\mathrm{Total}})$	97.4	97.4	%	0.035%

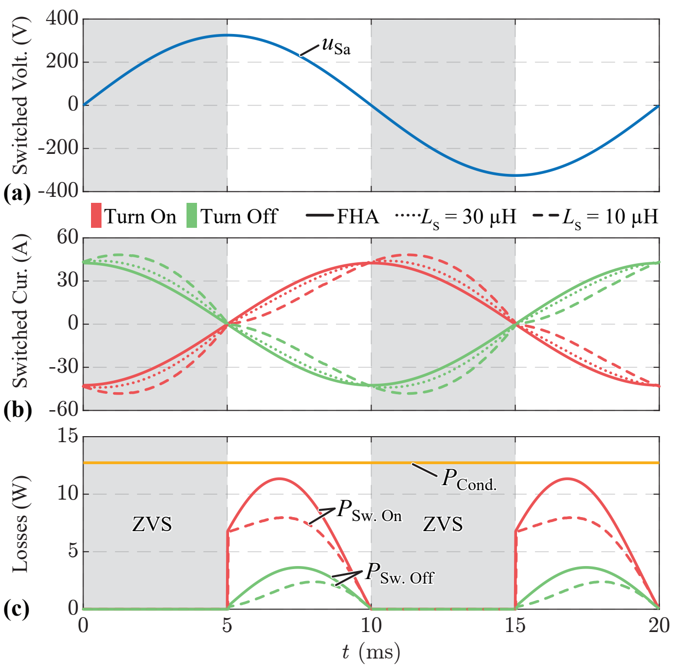

Fig. 7. Switching loss analysis of the $20\,\mathrm{m\Omega}$ M-BDS device S_{a} with zero voltage switching regions highlighted. The switching losses are evaluated with the switched current at turn on (red) and turn off (green). Solid lines represent the behaviour based on the FHA while the dotted and dashed lines represent simulation results with $L_{\mathrm{S}} = 30\,\mu\mathrm{H}$ and $L_{\mathrm{S}} = 10\,\mu\mathrm{H}$, respectively. Simulation results indicate that switching losses are improved with a low inductance value (lower attenuation of higher harmonics).

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