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***Abstract*—This paper proposes a new phase current balancing control method for multi-phase full-bridge step-down dc-dc converters with bipolar output voltage, targeting cryogenic ultra-low-loss power supplies for high-temperature-superconducting (HTS) magnet systems of future particle accelerators. Achieving ultra-low losses requires balanced average phase currents but prohibits the use of dedicated phase current sensors or shunts. Therefore, the proposed method reconstructs the phase current imbalance information by indirectly sensing the dc input capacitor current via the dv/dt and processing it in the frequency domain with low computational complexity. Compared to similar existing methods that only target half-bridge dc-dc step-down converters, the proposed method supports full-bridge topologies and high phase counts, as confirmed by detailed circuit simulations with 12 full-bridge phase modules. Finally, the balancing can be improved by phase inductance estimates based on indirectly sensing the output capacitor current, and carrier-to-phase reassignment utilizing the balancing controller information ensures optimum ripple cancellation at the output.**

***Index Terms*—Cryogenic power electronics, multi-phase converters, phase current balancing, full-bridge converters.**

I. Introduction

To enable new discoveries in physics, the feasibility of a new large-scale particle accelerator, the future circular collider (FCC), with a circumference of 80-100 km, about three times that of the Large Hadron Collider (LHC) at CERN in Geneva, Switzerland, is currently being studied [1]. Particle accelerators require various types of very strong electromagnets for guiding the particle beams. Aiming at minimizing the FCC's energy consumption, state-of-the-art room-temperature normal-conducting magnets (with high conduction losses) or low-temperature-superconducting magnets (with high power requirement of the cooling systems) should be replaced by high-temperature-superconducting (HTS) magnet systems. Still, the thick current leads connecting an HTS magnet, which resides in a cryostat, with the outside power supply unit (PSU), lead to a significant heat leak-in and a corresponding power demand of the cryocoolers. If instead a dc-dc step-down converter is placed inside of the magnet's cryostat, i.e., operates at around 70 K as indicated in **Fig. 1a**, the current leads can be designed for a much lower current and hence the leak-in losses are reduced. On the other hand, targeting a reduction of the cryocooler heat load by a factor of 4 compared to the state of the art with thick current leads, the loss budget for the cryogenic dc-dc step-down converter is very tight (specifically, < 5 W for a magnet current of 250 A) [2].

To enable low conduction losses and four-quadrant operation, a full-bridge multi-phase step-down converter topology as shown in **Fig. 1b** is selected [2]. Ensuring minimum losses further requires an equal load current sharing among the converter phases. However, phase-to-phase mismatches of up to $\pm 10\%$ for the phase inductances and up to $\pm 50\%$ for the transistors' on-state resistances must be expected, which cause phase current imbalances in practical multi-phase converter realizations, and thus closed-loop control of the (average) phase-currents is needed [3]–[9].

Literature discusses various implementation options, mainly targeting half-bridge-type dc-dc step-down converters without bipolar output voltage capability, e.g., for CPU voltage regulator modules. Typically, each phase current is measured using dedicated current sensors, dedicated shunt resistors or via the low-frequency (resistive) voltage drop across the phase inductors [3]; however, the tight loss budget of the considered application requires that any series resistances are minimized. Thus, also passive balancing mechanisms requiring zero-

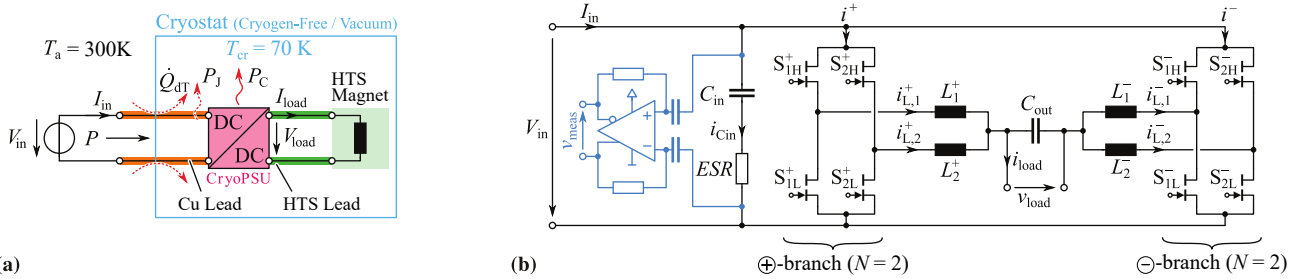

Fig. 1. (a) Concept of a cryogenic power supply for high-temperature-superconducting (HTS) magnets, where an ultra-low-loss dc-dc step-down converter operates inside of the magnet's cryostat at 70 K. **(b)** Considered full-bridge multi-phase dc-dc step-down converter topology with a simplified representation of the indirect input capacitor current sensing circuit (based on measuring the capacitor voltage dv/dt) needed for the proposed phase current balancing method. Note that only $N = 2$ phases per branch are shown to facilitate the explanations (see **Fig. 2** for key waveforms); practical realizations feature more phases depending on the loss budget and the rated magnet current.

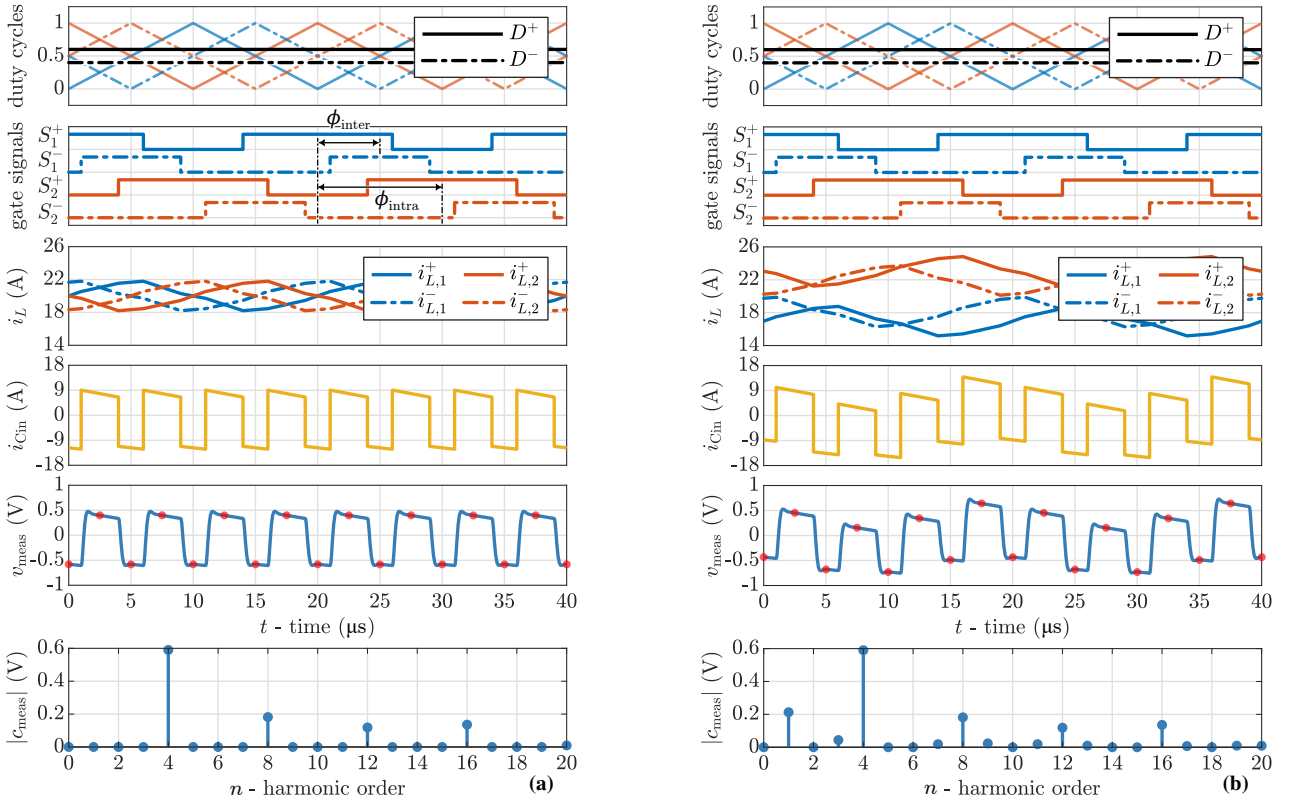

Fig. 2. Key waveforms of the full-bridge multi-phase dc-dc step-down converter from **Fig. 1b** with $N = 2$ phases, a switching frequency of $f_{\text{sw}} = 50\,\text{kHz}$, an input voltage of $V_{\text{in}} = 1\,\text{V}$, and a dc load current of $I_{\text{load}} = 40\,\text{A}$; further, $D^+ = D_{\text{CM}} + D_{\text{DM}}$ and $D^- = D_{\text{CM}} - D_{\text{DM}}$ are the duty cycles of the ⊕- and ⊖-branch (see **Fig. 1b**), where $D_{\text{CM}} = 0.5$ is the CM duty cycle and D_{DM} is the DM duty cycle that defines the output voltage. **(a)** Fully symmetric conditions and hence equal current sharing (i.e., equal average values of all phase inductor currents i_{L}) and **(b)** considering component mismatches and hence unequal current sharing among the phases, which affects the dc input capacitor current i_{Cin} and thus the time-domain waveform and the spectrum of the sensing circuit's output voltage v_{meas} (note that the harmonic order $n = 1$ corresponds to the device switching frequency f_{sw}). The sampling instants of v_{meas} (with $f_{\text{sample}} = 2 \cdot 2N f_{\text{sw}}$) that are used by the proposed balancing controller from **Fig. 4** are indicated by red dots (•).

voltage-switching (ZVS) designs [4], [5] with (approximately) 30% higher conduction losses are not applicable. Alternatively, the phase currents could be reconstructed using a single current sensor on the dc input side and the switching state information [7], [8]; these methods are, however, only feasible for low duty-cycles ($D \leq \frac{1}{2N}$) or converters with a low phase count N due to the computational complexity of the involved matrix inversions.

Finally, as indicated in **Fig. 2**, the dc input capacitor current (and/or voltage ripple) contains the phase current information. As proposed for a half-bridge multi-phase buck converter in [9], the indirectly (via the capacitor voltage $\mathrm{d}v/\mathrm{d}t$) sensed input capacitor current can be processed in the frequency domain to extract the phase current imbalance information (if not the absolute values). However, the approach from [9] is limited to a half-bridge topology with unipolar output voltage only, to a narrow operating range (e.g., output voltage/current) or a fixed operating point, depends on the equivalent series resistance (ESR) of the input capacitor, and the robustness as well as the implementation with a large number of interleaved phases (e.g., $N > 8$) has not been demonstrated so far.

Therefore, this work proposes a new extended/improved phase current balancing method for full-bridge multi-phase dc-dc converters (see **Fig. 1b**) based on the processing of the indirectly sensed input dc capacitor current in the frequency domain. The method supports a wide operating range, a high phase count (e.g., $N > 8$) and shows low dependency on the input dc capacitor's equivalent series resistance (ESR). In the following, **Section II** first discusses the optimum modulation scheme of full-bridge multi-phase converters before **Section III** introduces the proposed phase current balancing method. **Section IV** discusses the implementation and improvement vectors, and **Section V** concludes the paper.

II. Converter Operation

The key converter waveforms are illustrated in **Fig. 2** for the case of $N = 2$ phases each in the ⊕-branch and in the ⊖-branch as shown in **Fig. 1**. The thus N individual carriers per branch are interleaved using the intra-branch interleaving angles of $\phi_{\text{intra}} = 2\pi/N \cdot (x-1)$ for $x \in [1, N]$. Furthermore, the carriers of the ⊕- and ⊖-branch are phase shifted by the inter-branch interleaving angle ϕ_{inter} against each other. The branch duty cycles D^+ and D^- follow from the desired common-mode (CM) and differential-mode (DM) voltage components at the output of the multi-phase full-bridge converter, i.e.,

$$D_{\text{CM}} = \frac{D^+ + D^-}{2} \quad \text{and} \quad D_{\text{DM}} = \frac{D^+ - D^-}{2}. \tag{1}$$

The DM duty-cycle D_{DM} is used to control the output voltage v_{load}, whereas the CM duty cycle D_{CM} and also the inter-phase interleaving angle ϕ_{inter} are degrees of freedom (DoF) that can

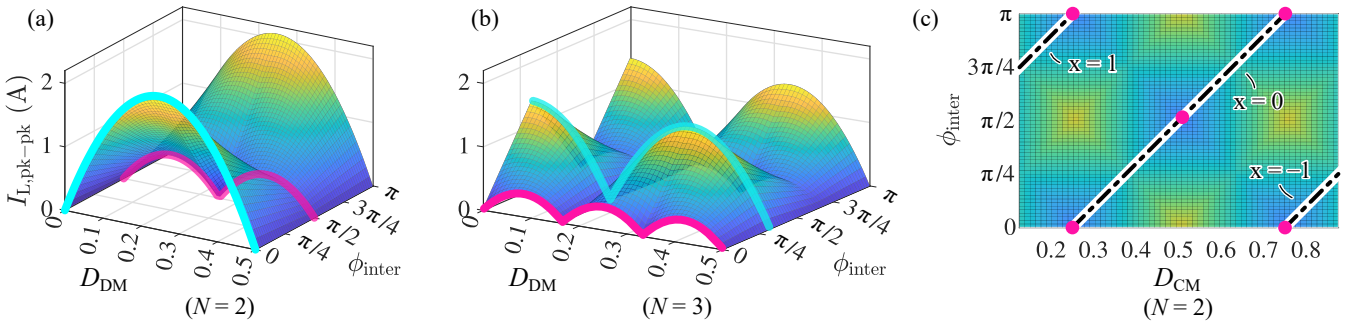

Fig. 3. Exemplary output current switching ripple cancellation depending on D_{DM} and the inter-branch interleaving angle ϕ_{inter} for a CM duty cycle of $D_{\mathrm{CM}} = 0.5$ and an **(a)** even number of $N = 2$ and **(b)** odd number of $N = 3$ phases; selecting the optimum ϕ_{inter} results in minimum output current ripple (•) compared to a suboptimal choice (•). **(c)** Optimum choice (resulting in minimum output current ripple) of the inter-branch interleaving angle ϕ_{inter} in dependence of the CM duty cycle D_{CM} for $N = 2$ and $D_{\mathrm{DM}} = 0.125$.

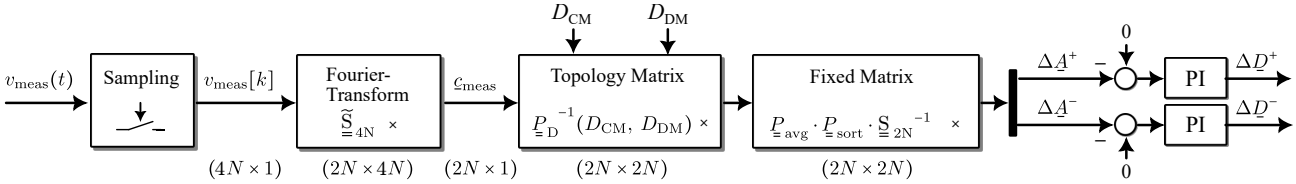

Fig. 4. Proposed closed-loop phase-current balancing controller for full-bridge multi-phase dc-dc converters as shown in **Fig. 1b**. The output signal of the indirect input capacitor current sensing circuit $v_{\mathrm{meas}}(t)$ is sampled (see **Fig. 2**) and processed in the frequency domain to obtain the phase current deviations $\Delta\underline{A}^+$ and $\Delta\underline{A}^-$ from the branch average, which are then controlled to zero by adapting the duty cycles of the individual half-bridges accordingly.

be adjusted for optimum ripple cancellation, see **Fig. 3ab**. D_{CM} is typically selected to maximize the available dynamic range for D_{DM} and the angle ϕ_{inter} is chosen to achieve an effective switching frequency (at the input and output) of $f_{\mathrm{eff}} = 2Nf_{\mathrm{sw}}$ and, thus, minimum required filtering effort. The optimum choices of the inter-branch interleaving angle ϕ_{inter} for a given D_{CM} for odd and even number of phases N are

$$\phi_{\mathrm{inter,opt.}}\Big|_{\text{odd N}} = \frac{2\pi}{N} \cdot x + (D_{\mathrm{CM}} - \frac{1}{2}) \cdot 2\pi \quad \text{and}$$
$$\phi_{\mathrm{inter,opt.}}\Big|_{\text{even N}} = \frac{2\pi}{2 \cdot N} \cdot (2x+1) + (D_{\mathrm{CM}} - \frac{1}{2}) \cdot 2\pi, \quad (2)$$

where $x \in \mathbb{Z}$, which is illustrated in **Fig. 3c**. To obtain $f_{\mathrm{eff}} = 2Nf_{\mathrm{sw}}$ at both the input and output, the CM duty-cycle in (2) should be chosen as $D_{\mathrm{CM}} = \frac{x}{2N}$ with $x \in [1, 2N-1]$, which is marked by the pink dots • in **Fig. 3c**.

Then, with respect to **Fig. 2**, the comparison of the duty-cycles D^+ and D^- for the ⊕- and ⊖-branches with the respective carrier signals results in the gate signals for the corresponding half-bridges. The phase inductor currents are balanced in the ideal case from **Fig. 2a** and the inductor current ripple cancels at both the input and the output as a result of the interleaved modulation. This ripple cancellation can also be observed in the input dc-link capacitor current waveform, which is indirectly sensed by measuring the input capacitor voltage $\mathrm{d}v/\mathrm{d}t$ with an active high-pass circuit as depicted in **Fig. 1**, i.e., the sensing circuit output voltage v_{meas} is proportional (adjustable via the gains of the measurement chain) to the (HF) dc-link capacitor current. Therefore, the ripple cancellation is visible in the harmonic spectrum v_{meas}, too. **Fig. 2b** depicts the same key waveforms for the case of unbalanced phase inductor currents, which result, e.g., from component mismatches like unequal on-state resistances amongst the transistors, etc. The unbalanced inductor currents imply non-ideal ripple cancellation at the input and output of the converter as can be seen in the input capacitor current waveform and the harmonic spectrum of v_{meas}; specifically, components between the device switching frequency f_{sw} and the effective switching frequency $f_{\mathrm{eff}} = 2Nf_{\mathrm{sw}}$ appear. The proposed phase current balancing controller uses these harmonics below f_{eff} in v_{meas} to determine the phase current unbalance, as explained in the following.

III. Phase Current Balancing Method

The core idea of the proposed method consists of equating analytical expressions (containing the phase current levels, the phase-specific carrier phase shifts, etc.) of the harmonic components (at the device switching frequency f_{sw} and higher) of the input capacitor current with the digitally computed harmonic spectrum of the sensed input capacitor current to calculate the phase current imbalance information, i.e., the deviations from the average phase current in each branch, $\Delta\underline{A}^+$ and $\Delta\underline{A}^-$ (the underline denotes a vector); this is similar to [9], where, however, only half-bridge topologies are considered.

Fig. 4 shows the block diagram of the closed-loop phase current balancing control implementation. Sensing the input capacitor voltage waveform with a properly designed analog signal conditioning circuit (see **Fig. 1b** and **Section IV-B**) yields a voltage signal v_{meas} whose harmonic spectrum is equivalent to that of the input capacitor current in the frequency range of interest. Thus, v_{meas} is sampled with a minimum sampling frequency of $f_{\mathrm{sample}} = 2 \cdot 2Nf_{\mathrm{sw}}$ to enable a reconstruction of $2N$ harmonic components below f_{eff}. The sample vector $v_{\mathrm{meas}}[k]$ is digitally processed with a truncated $4N$-point discrete Fourier transform (DFT) $\underline{\tilde{S}}_{4N}$ to extract the complex spectrum $\underline{c}_{\mathrm{meas}}$ (i.e., amplitude and phase of the harmonics) containing $2N$ harmonics.

The key challenge lies then in solving the resulting system of equations for the phase current imbalance information $\Delta\underline{A}^+$ and $\Delta\underline{A}^-$, which requires a suitable modification of the equations to obtain a simple formulation and low computational effort for a microcontroller implementation, which is discussed in detail in **Section III-A**. Finally, low-bandwidth PI controllers are used to equalize the phase currents in each branch by applying minor modifications to the duty cycles of the individual bridge-legs.

A. Phase Current Unbalance Estimation

The input capacitor current $i_{\mathrm{Cin}} = I_{\mathrm{in}} - (i^+ + i^-)$ is composed of a dc component supplied from the input terminal (assuming sufficient impedance towards the feeding source, see **Section IV-A**) and of two pulsed current contributions from the multi-phase buck $\oplus$- and $\ominus$-branches. The pulsed currents i^+ and i^- are comprised of the respective phase inductor currents $i^+_{\mathrm{L},1}$, $i^+_{\mathrm{L},2}$, …, $i^+_{\mathrm{L,N}}$ and $i^-_{\mathrm{L},1}$, $i^-_{\mathrm{L},2}$, …, $i^-_{\mathrm{L,N}}$ according to

$$i^+ = \sum_{i=1}^{N} s_{\mathrm{i}}^+ \cdot i^+_{\mathrm{L,i}} \quad \text{and} \quad i^- = \sum_{i=1}^{N} s_{\mathrm{i}}^- \cdot i^-_{\mathrm{L,i}}, \tag{4}$$

where s_{i}^+ and s_{i}^- denote the switching state of the i-th bridge-leg of the $\oplus$- and $\ominus$-branch respectively. Following the general idea of [9], the complex-valued Fourier coefficients of the input capacitor current are

$$\begin{aligned}(\underline{c}_{\mathrm{iCin}})_{\mathrm{k}} &= (\underline{c}_{\mathrm{I_{DC}}})_{\mathrm{k}} \\ &- \underbrace{\frac{\sin(k\cdot\pi\cdot D_+)}{k\cdot\pi}}_{\underline{\underline{K}}^+} \cdot \sum_{m=0}^{N-1} \Big(\underbrace{e^{-j\cdot\frac{2\pi\cdot k\cdot m}{N}}}_{\underline{\underline{S}}_{\mathrm{N}}} \cdot \underbrace{(A^+)_{\mathrm{m}}}_{\underline{A}^+} \Big) \\ &+ \underbrace{e^{-j\cdot k\cdot\phi_{\mathrm{inter}}}}_{\underline{\underline{K}}^{\phi}} \cdot \underbrace{\frac{\sin(k\cdot\pi\cdot D_-)}{k\cdot\pi}}_{\underline{\underline{K}}^-} \cdot \sum_{m=0}^{N-1} \Big(\underbrace{e^{-j\cdot\frac{2\pi\cdot k\cdot m}{N}}}_{\underline{\underline{S}}_{\mathrm{N}}} \cdot \underbrace{(A^-)_{\mathrm{m}}}_{\underline{A}^-} \Big),\end{aligned} \tag{5}$$

where $k \in \mathbb{N}_0$, $\underline{c}_{\mathrm{I_{DC}}}$ denotes the dc component resulting from the input side dc current I_{in}, $(A^+)_{\mathrm{m}}$ and $(A^-)_{\mathrm{m}}$ represent the average inductor currents of the $(m+1)$-th phase for the $\oplus$- and $\ominus$-branch respectively. As indicated below the braces in (5), the sum of the pulsed current contributions from the branches can be rewritten in matrix-vector notation by using the diagonal matrices $\underline{\underline{K}}^+$, $\underline{\underline{K}}^-$ and $\underline{\underline{K}}^{\phi}$, and the N-point DFT matrix $\underline{\underline{S}}_{\mathrm{N}}$. Note that $\underline{c}_{\mathrm{I_{DC}}} = [c_{\mathrm{I_{DC}},0}, 0, \ldots, 0]^T$ contains only a dc component, which cancels out in the final result (11) when carried through, and for simplicity will be disregarded already from this point on. The same applies to the ac ripple components of the phase currents as long as equal phase inductances are considered (see also **Section IV-C**).

The obtained matrix-vector equation (5) contains $2N$ unknown average phase current values in total (N unknown currents $\underline{A}^+$ and $\underline{A}^-$ for the two branches, respectively), which appear, however, in pairs (as sums). Therefore, (5) provides only N equations (i.e., only N Fourier coefficients are considered) to solve for these $2N$ unknowns. In principle, however, more than N harmonics could be considered to increase the number of equations as needed. This can be elegantly implemented by combining the unknown $(N \times 1)$ vectors $\underline{A}^+$ and $\underline{A}^-$ conveniently by stagger-arranging the phase currents into a composite vector $\underline{A} = [A^+_1,\ A^-_1,\ A^+_2,\ A^-_2,\ \ldots]^T$, introducing the masking matrices[1] $\underline{\underline{M}}^+$ and $\underline{\underline{M}}^-$, and extending the N-point DFT matrix $\underline{\underline{S}}_{\mathrm{N}}$ to a $2N$-point DFT matrix $\underline{\underline{S}}_{\mathrm{2N}}$:

$$\begin{aligned}\underline{c}_{\mathrm{iCin}} &= -\underline{\underline{K}}^+ \cdot \underbrace{\underline{\underline{S}}_{\mathrm{N}} \cdot \underline{A}^+}_{\substack{=\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{\underline{M}}^+\cdot\underline{A} \\ =\underline{\underline{T}}^+\cdot\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{A}}} + \underline{\underline{K}}^{\phi}\cdot\underline{\underline{K}}^- \cdot \underbrace{\underline{\underline{S}}_{\mathrm{N}} \cdot \underline{A}^-}_{\substack{=\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{\underline{M}}^-\cdot\underline{A} \\ =\underline{\underline{T}}^-\cdot\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{A}}} \\ &= -\underline{\underline{K}}^+\cdot\underline{\underline{T}}^+\cdot\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{A} + \underline{\underline{K}}^{\phi}\cdot\underline{\underline{K}}^-\cdot\underline{\underline{T}}^-\cdot\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{A} \\ &= \underbrace{(-\underline{\underline{K}}^+\cdot\underline{\underline{T}}^+ + \underline{\underline{K}}^{\phi}\cdot\underline{\underline{K}}^-\cdot\underline{\underline{T}}^-)}_{=\underline{\underline{P}}_{\mathrm{D}}}\cdot\underline{\underline{S}}_{\mathrm{2N}}\cdot\underline{A}\end{aligned} \tag{6}$$

The final rearrangement advantageously features a conveniently invertible matrix on the right-hand side, i.e., the product of the unitary $2N$-point DFT matrix $\underline{\underline{S}}_{\mathrm{2N}}$ and a (2×2) block-diagonal matrix $\underline{\underline{P}}_{\mathrm{D}}$, which we will refer to as *topology matrix* in the following. The topology matrix $\underline{\underline{P}}_{\mathrm{D}}$ is given in (3) at the bottom of the page, and its entries are:

$$\begin{aligned}(k_1^+)_{\mathrm{kk}} &= \frac{\sin(k\cdot\pi\cdot D^+)}{k\cdot\pi} & (k_2^+)_{\mathrm{kk}} &= \frac{\sin((k+N)\cdot\pi\cdot D^+)}{(k+N)\cdot\pi} \\ (k_1^-)_{\mathrm{kk}} &= \frac{\sin(k\cdot\pi\cdot D^-)}{k\cdot\pi} & (k_2^-)_{\mathrm{kk}} &= \frac{\sin((k+N)\cdot\pi\cdot D^-)}{(k+N)\cdot\pi} \\ (k_1^{\phi})_{\mathrm{kk}} &= e^{-i\cdot k\cdot\phi_{\mathrm{inter}}} & (k_2^{\phi})_{\mathrm{kk}} &= e^{-i\cdot(k+N)\cdot\phi_{\mathrm{inter}}} \\ (w)_{\mathrm{kk}} &= e^{i\cdot\frac{\pi}{N}\cdot k}.\end{aligned} \tag{7}$$

Solving for the phase current average information yields

$$\begin{aligned}\underline{A} &= \underline{\underline{S}}_{\mathrm{2N}}{}^{-1}\cdot\underline{\underline{P}}_{\mathrm{D}}{}^{-1}\cdot\underline{c}_{\mathrm{meas}} \\ &= \underline{\underline{S}}_{\mathrm{2N}}{}^{-1}\cdot\underline{\underline{P}}_{\mathrm{D}}{}^{-1}\cdot(\widetilde{\underline{\underline{S}}}_{\mathrm{4N}}\cdot\underline{v}_{\mathrm{meas}}),\end{aligned} \tag{8}$$

[1]These are necessary to map the correct columns of $\underline{\underline{S}}_{\mathrm{2N}}$ with the corresponding entries/rows of $\underline{A}$.

$$\begin{aligned}\underline{\underline{P}}_{\mathrm{D}} &= -\underbrace{\left(\begin{array}{c|c}\underline{\underline{K}}_1^+ & 0 \\ \hline 0 & \underline{\underline{K}}_2^+\end{array}\right)}_{\underline{\underline{K}}^+}\cdot\frac{1}{2}\underbrace{\left(\begin{array}{c|c}\underline{\underline{I}} & \underline{\underline{I}} \\ \hline \underline{\underline{I}} & \underline{\underline{I}}\end{array}\right)}_{\underline{\underline{T}}^+} + \underbrace{\left(\begin{array}{c|c}\underline{\underline{K}}_1^{\phi} & 0 \\ \hline 0 & \underline{\underline{K}}_2^{\phi}\end{array}\right)}_{\underline{\underline{K}}^{\phi}}\cdot\underbrace{\left(\begin{array}{c|c}\underline{\underline{K}}_1^- & 0 \\ \hline 0 & \underline{\underline{K}}_2^-\end{array}\right)}_{\underline{\underline{K}}^-}\cdot\frac{1}{2}\underbrace{\left(\begin{array}{c|c}\underline{\underline{W}} & -\underline{\underline{W}} \\ \hline \underline{\underline{W}} & -\underline{\underline{W}}\end{array}\right)}_{\underline{\underline{T}}^-} \\ &= -\frac{1}{2}\cdot\left(\begin{array}{c|c}\underline{\underline{K}}_1^+ - \underline{\underline{K}}_1^-\cdot\underline{\underline{K}}_1^{\phi}\cdot\underline{\underline{W}} & \underline{\underline{K}}_1^+ + \underline{\underline{K}}_1^-\cdot\underline{\underline{K}}_1^{\phi}\cdot\underline{\underline{W}} \\ \hline \underline{\underline{K}}_2^+ - \underline{\underline{K}}_2^-\cdot\underline{\underline{K}}_2^{\phi}\cdot\underline{\underline{W}} & \underline{\underline{K}}_2^+ + \underline{\underline{K}}_2^-\cdot\underline{\underline{K}}_2^{\phi}\cdot\underline{\underline{W}}\end{array}\right) =: -\frac{1}{2}\cdot\left(\begin{array}{c|c}\underline{\underline{X}} & \underline{\underline{U}} \\ \hline \underline{\underline{V}} & \underline{\underline{Y}}\end{array}\right)\end{aligned} \tag{3}$$

where $\underline{c}_{\mathrm{meas}} = \underline{\underline{\widetilde{S}}}_{4\mathrm{N}} \cdot \underline{v}_{\mathrm{meas}}$ denotes the discrete complex spectrum of the sensing circuit output voltage.[2] Advantageously, the inverse of the (2×2) block diagonal topology matrix $\underline{\underline{P}}_{\mathrm{D}}$ can be evaluated analytically [10] as

$$\underline{\underline{P}}_{\mathrm{D}}{}^{-1} = \frac{-2}{(X)_{\mathrm{kk}}(Y)_{\mathrm{kk}} - (U)_{\mathrm{kk}}(V)_{\mathrm{kk}}} \left(\begin{array}{c|c} (Y)_{\mathrm{kk}} & -(U)_{\mathrm{kk}} \\ \hline -(V)_{\mathrm{kk}} & (X)_{\mathrm{kk}} \end{array} \right), \quad (9)$$

with $k \in [0, N-1]$ and where

$$\begin{aligned} (X)_{\mathrm{kk}} &= (k_1^+)_{\mathrm{kk}} - (k_1^-)_{\mathrm{kk}} \cdot (k_1^\phi)_{\mathrm{kk}} \cdot (w)_{\mathrm{kk}} \\ (U)_{\mathrm{kk}} &= (k_1^+)_{\mathrm{kk}} + (k_1^-)_{\mathrm{kk}} \cdot (k_1^\phi)_{\mathrm{kk}} \cdot (w)_{\mathrm{kk}} \\ (V)_{\mathrm{kk}} &= (k_2^+)_{\mathrm{kk}} - (k_2^-)_{\mathrm{kk}} \cdot (k_2^\phi)_{\mathrm{kk}} \cdot (w)_{\mathrm{kk}} \\ (Y)_{\mathrm{kk}} &= (k_2^+)_{\mathrm{kk}} + (k_2^-)_{\mathrm{kk}} \cdot (k_2^\phi)_{\mathrm{kk}} \cdot (w)_{\mathrm{kk}}. \end{aligned} \quad (10)$$

Note that the $k = 0$ entry of each of the four diagonal matrices needs to be evaluated analytically by using L'Hôpital's rule. The numerical conditioning of the inverse topology matrix $\underline{\underline{P}}_{\mathrm{D}}{}^{-1}$ is further discussed in **Section III-C**. Finally, two auxiliary linear transformations, $\underline{\underline{P}}_{\mathrm{sort}}$ to sort the aggregate vector $\underline{A}$ in order to obtain $[\underline{A}^+, \underline{A}^-]^T$ and $\underline{\underline{P}}_{\mathrm{avg}}$ in order to have a relative measure for the phase current variations in each of the two branches, are used to finally obtain the relative deviations $\Delta\underline{A}$ of the individual phase currents from the branch-level mean values as

$$\begin{aligned} \Delta\underline{A} &= \left[\begin{array}{c} \Delta\underline{A}^+ \\ \Delta\underline{A}^- \end{array} \right] \\ &= \underbrace{\underline{\underline{P}}_{\mathrm{avg}} \cdot \underline{\underline{P}}_{\mathrm{sort}} \cdot \underline{\underline{S}}_{2\mathrm{N}}{}^{-1}}_{\underline{\underline{\mathrm{Left}}}} \cdot \underline{\underline{P}}_{\mathrm{D}}{}^{-1} \cdot (\underline{\underline{\widetilde{S}}}_{4\mathrm{N}} \cdot \underline{v}_{\mathrm{meas}}). \end{aligned} \quad (11)$$

Advantageously, the matrix $\underline{\underline{\mathrm{Left}}}$ is constant and the inverse of the topology matrix $\underline{\underline{P}}_{\mathrm{D}}^{-1}$ must only be updated when the duty cycles change, i.e., for the required relatively slow phase current balancing in steady-state, the computational burden is moderate. As indicated in **Fig. 4**, PI controllers then ultimately regulate the deviations $\Delta\underline{A}$ to zero.

B. Small D_{DM} Approximation

For small (i.e., $< 1\%$) values of D_{DM}, which is, for example, the case in the considered HTS magnet application,[3] the computations in equation (9) can be simplified to minimize the computational effort by using

$$\begin{aligned} \sin(k\pi D^+) = &\sin(k\pi D_{\mathrm{CM}})\cos(k\pi D_{\mathrm{DM}}) \\ &+ \sin(k\pi D_{\mathrm{DM}})\cos(k\pi D_{\mathrm{CM}}) \approx \sin(k\pi D_{\mathrm{CM}}) \end{aligned} \quad (12)$$

and likewise for $\sin(k\pi D^-)$, $\sin\big((k+N)\pi D^+\big)$, and $\sin\big((k+N)\pi D^-\big)$. This results in a simplified inverse for the topology matrix as

$$\underline{\underline{P}}_{\mathrm{D}}{}^{-1}\Big|_{\text{small } D_{\mathrm{DM}}} = \left(\begin{array}{c|c} (E)_{\mathrm{kk}} & (F)_{\mathrm{kk}} \\ \hline (G)_{\mathrm{kk}} & (H)_{\mathrm{kk}} \end{array} \right), \quad (13)$$

with $k \in [0, N-1]$ and where

$$\begin{aligned} (E)_{\mathrm{kk}} &= \frac{-k\pi}{2(c-1)} \cdot \frac{e^{ik\left(\phi_{\mathrm{inter}} - \frac{\pi}{N}\right)} + c}{\sin(k\pi D_{\mathrm{CM}})} \\ (F)_{\mathrm{kk}} &= \frac{(k+N)\pi}{2(c-1)} \cdot \frac{e^{ik\left(\phi_{\mathrm{inter}} - \frac{\pi}{N}\right)} + 1}{\sin\big((k+N)\pi D_{\mathrm{CM}}\big)} \\ (G)_{\mathrm{kk}} &= \frac{k\pi}{2(c-1)} \cdot \frac{e^{ik\left(\phi_{\mathrm{inter}} - \frac{\pi}{N}\right)} - c}{\sin(k\pi D_{\mathrm{CM}})} \\ (H)_{\mathrm{kk}} &= \frac{-(k+N)\pi}{2(c-1)} \cdot \frac{e^{ik\left(\phi_{\mathrm{inter}} - \frac{\pi}{N}\right)} - 1}{\sin\big((k+N)\pi D_{\mathrm{CM}}\big)} \\ c &= e^{-iN\phi_{\mathrm{inter}}}. \end{aligned} \quad (14)$$

Again, the first element $(k = 0)$ of each diagonal matrix in the (2×2) block-diagonal matrix must be calculated with L'Hôpital's rule. Compared with the general expression in (9), where six trigonometric function evaluations per entry of the block-diagonal matrix are needed, the approximation requires the computation of only a single sine function per entry, with a corresponding reduction of the computational burden.

C. Robust Numerical Implementation

For the inverse of the topology matrix $\underline{\underline{P}}_{\mathrm{D}}$ to exist, the following two general conditions have to be met [10]:

- $\underline{\underline{X}}$ is non-singular, and
- $\underline{\underline{Y}} - \underline{\underline{V}} \cdot \underline{\underline{X}}^{-1} \cdot \underline{\underline{U}}$ is invertible.

This implies that a few discrete combinations of CM and DM duty cycles should be avoided, e.g., for $N = 2$ this would be the combinations $(D_{\mathrm{CM}} = \frac{3}{4},\ D_{\mathrm{DM}} = \frac{1}{4})$ and $(D_{\mathrm{CM}} = \frac{2}{3},\ D_{\mathrm{DM}} = \frac{1}{3})$; the same applies to certain discrete branch duty cycle values D^+ and D^-.[4]

In case of the approximation for small DM duty cycles D_{DM}, ensuring that both conditions above are satisfied and, thus, the entries of $\underline{\underline{P}}_{\mathrm{D}}{}^{-1}\Big|_{\text{small } D_{\mathrm{DM}}}$ are non-singular, i.e., the argument of the sine functions in the denominators does not equal an integer multiple of π, only the following CM duty cycles

$$D_{\mathrm{CM}} = \frac{1}{x} \quad \text{for } x \in \Big[2, 2N\Big], \quad (15)$$

must be avoided, e.g., for $N = 2$ this would be the CM duty cycles $D_{\mathrm{CM}} = \frac{1}{2}, \frac{1}{3}$ and $\frac{1}{4}$. Choosing a CM duty cycle that

[2]This can be obtained by using the 4N-point DFT $\underline{\underline{\widetilde{S}}}_{4\mathrm{N}}$, or alternatively with a fast Fourier transformation (FFT). Note that v_{meas} is proportional to the dc-link capacitor $\mathrm{d}v/\mathrm{d}t$ and hence the capacitor current; as finally only the current deviations are of interest, absolute values are not required.

[3]HTS magnet load with residual resistance in the order of $1\,\mu\Omega$, $250\,\mathrm{A}$ load current and $1\,\mathrm{V}$ dc input voltage result in $D_{\mathrm{DM}} \approx 0.0125\%$.

[4]Specifically, these are

$$\left(D_{\mathrm{CM}} = \frac{\frac{1}{x} + \frac{1}{y}}{2},\quad D_{\mathrm{DM}} = \frac{\frac{1}{x} - \frac{1}{y}}{2}\right), \text{ with}$$

$$x \in \Big[1, x_{\max} = \Big\lfloor \frac{\sqrt{8N-3}-1}{2} \Big\rfloor\Big] \text{ and } y \in \Big[x+1, \Big\lfloor \frac{2}{x}N - 1 \Big\rfloor\Big],$$

and

$$\begin{aligned} D^{+/-} &= \frac{1}{3},\ \frac{2}{3} \text{ and } 1 && \text{for odd (non-prime) } N > 3, \\ D^{+/-} &= \frac{1}{N} \cdot 2x \ \text{ with } x \in \Big[1, \frac{N}{2}\Big] && \text{for even } N, \end{aligned}$$

for even N that are divisible by 3, additionally:

$$D^{+/-} = \frac{3}{N} \cdot (2x+1) \ \text{ with } x \in \Big[0, \frac{N}{6} - 1\Big].$$

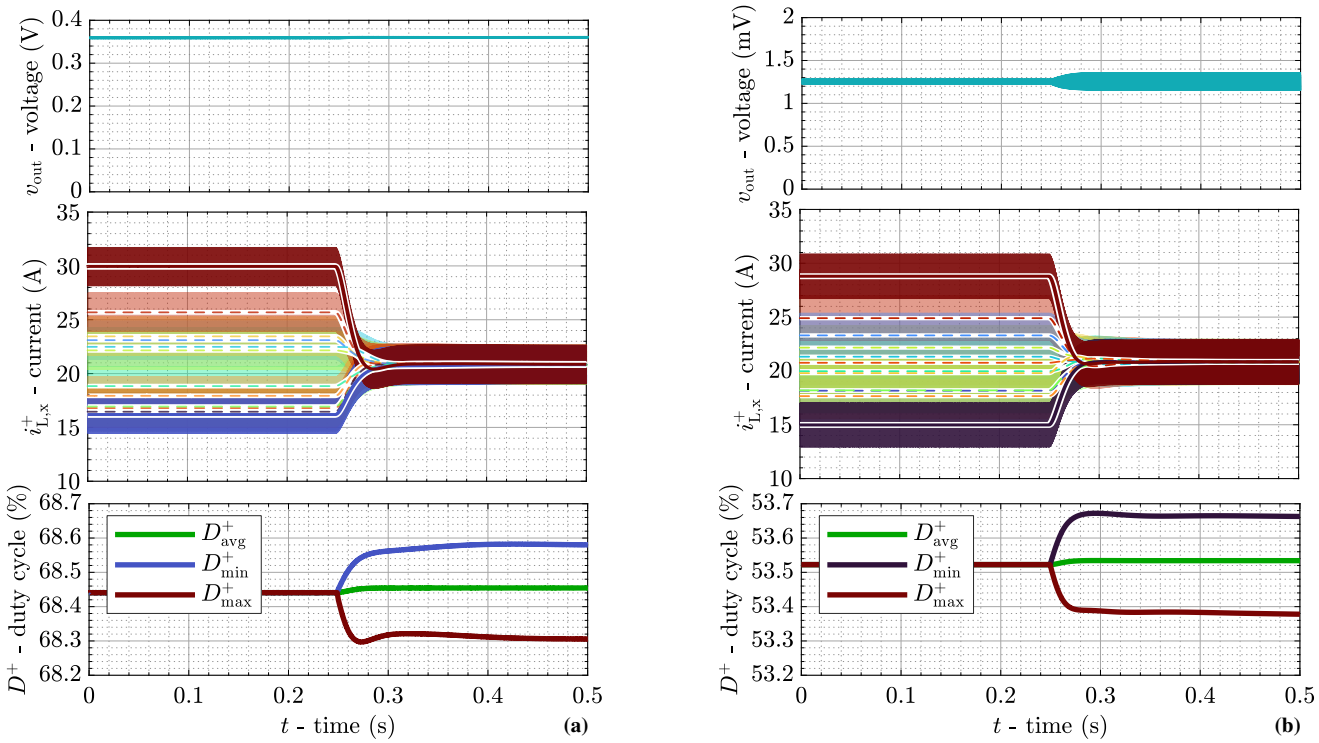

Fig. 5. Simulation results for a converter design with $N = 12$ full-bridge phase modules, $V_{\text{in}} = 1\,\text{V}$, $f_{\text{sw}} = 50\,\text{kHz}$, phase inductances $L^+_{\text{x}} = L^-_{\text{x}} = 1.2\,\mu\text{H}$, and up to $\pm 50\%$ phase-to-phase mismatches of the transistors' on-state resistances for two operating points, i.e., **(a)** $D_{\text{CM}} = 50\%$ and $D_{\text{DM}} = 18\%$ and **(b)** $D_{\text{CM}} = 53\%$ and $D_{\text{DM}} = 0.0625\%$ which allows to employ the simplified computations for small DM duty cycles. The balancing controller is activated at $t = 0.25\,\text{s}$ and adjusts the duty cycles of the individual phases D^+_{x} and D^-_{x} with $x = 1 \dots N$ for the $\oplus$-branch and $\ominus$-branch respectively; only the minimum, maximum and average duty cycle of the $\oplus$-branch are shown for better visibility.

is close to these values is not problematic as long as a small margin of, e.g., 1% is kept.

In general, the CM duty cycle is a DoF in many applications and thus the "critical" CM, DM, or branch duty cycles can typically be avoided with minor adjustments of D_{CM}. Furthermore, operation with many of the critical duty cycles is still possible, if the resulting singular entries of the topology matrix are avoided by replacing the respective rows (i.e., equations) with equations using higher-order harmonics. The choice of higher order harmonics is important such that the derived equations in (11) and (18) stay unchanged apart for the few block-diagonal entries in the (inverse) topology matrix. Specifically, a harmonic of order $k_{\text{new}} = k+2N$ should be used instead of a critical (i.e., singular) k-th entry in the original topology matrix, because the entries of the $2N$-point DFT matrix $\underline{\underline{S}}_{2\text{N}}$ repeat every $2N$ rows again, thus, $\underline{\underline{S}}_{2\text{N}}$ would keep its unitary property and in this case even remains unchanged. Apart from modifying the entries of a few rows of the inverse topology matrix, only the corresponding rows of the truncated $4N$-point DFT matrix $\underline{\underline{\widetilde{S}}}_{4\text{N}}$ must be replaced to extract the required new harmonics with order k_{new} from $\underline{v}_{\text{meas}}$.

D. Simulation Results

The proposed phase current balancing method is verified by closed-loop simulation results of a full-bridge dc-dc step-down converter as shown in **Fig. 1b** but with $N = 12$ full-bridge phase modules (i.e., 24 half-bridges in total). Large phase-to-phase mismatches of the transistor on-state resistances $R_{\text{ds(on)}}$ of up to $\pm 50\%$ have been introduced (with a random distribution), resulting in a wide variation of the average phase currents before the controller is activated at $t = 0.25\,\text{s}$ in **Fig. 5ab**. Whereas in **Fig. 5a**, $D_{\text{CM}} = 50\%$ and $D_{\text{DM}} = 18\%$ require the full computations with (9), **Fig. 5b** considers $D_{\text{CM}} = 53\%$ and $D_{\text{DM}} = 0.0625\%$ (e.g., assuming a $5\,\mu\Omega$ parasitic resistance of an HTS magnet load) and thus the small D_{DM} approximation (with lower computational effort) from (13) is employed. In both cases, the proposed balancing method achieves almost perfect current sharing among the phases. However, the output voltage quality could be adversely affected by the then (necessarily) unequal duty cycles of the half-bridges, as is evident from the increase of the output voltage ripple observed in **Fig. 5b** (**Section IV-D** discusses carrier-phase reordering as a countermeasure).

IV. Implementation and Improvement Vectors

In the following, a few important aspects regarding the implementation of the sensing circuitry, and two possibilities for improving the overall system performance are briefly discussed.

A. Input-Side Decoupling Impedance

Considering the power circuit from **Fig. 1b**, it is important to note that most of the pulsed switching ripple current from the $\oplus$- and $\ominus$-branches should close through the bulk dc-link capacitor, whose $\text{d}v/\text{d}t$ is sensed and used for estimating the phase current unbalance. This requires that any upstream converter unit that provides the dc input voltage has either

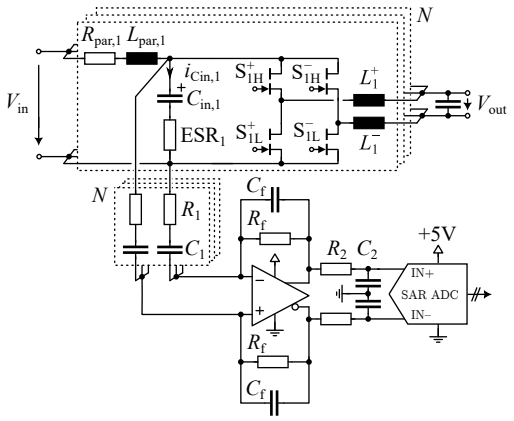

Fig. 6. Indirect input capacitor current sensing circuit for distributed (e.g., amongst full-bridge phase modules) dc-link capacitors.

sufficient output impedance or the interconnection impedance is sufficiently large. A rule of thumb can be provided based on a worst-case allowable ripple current share of $x_{\text{L,in}} \approx 5 \ldots 10\%$ not flowing through the dc-link capacitor. Then, assuming zero output impedance of the upstream converter, a decoupling inductance of

$$L_{\text{input}} \geq \frac{1}{\omega^2} \cdot \frac{1}{C_{\text{in}}} \cdot \frac{1 - x_{\text{L,in}}}{x_{\text{L,in}}} \tag{16}$$

at the first switching harmonic with $\omega = 2\pi \cdot f_{\text{sw}}$ is required.

B. Sensing Circuit for Distributed DC-Link Capacitors

The circuit that is used for indirectly sensing the input capacitor current waveform is depicted in **Fig. 6**. In contrast to the simplified variant from **Fig. 1**, the case of a distributed dc-link capacitor bank, as often found in phase-modular designs of multi-phase converters, is considered. The individual dc-link capacitor $\mathrm{d}v/\mathrm{d}t$ are measured using dedicated R_1C_1 branches summed up at a fully-differential amplifier, which is configured as an active high-pass filter with R_1 and C_{f} utilized as high-frequency roll-off components; R_2 and C_2 form an anti-aliasing filter at the input of the differential analog-to-digital converter (ADC). Reconstructing the required $2N$ harmonics below f_{eff} used for the phase current estimation requires a measurement bandwidth of at least $\text{BW} = 2 \cdot 2N f_{\text{sw}}$. For a converter design with $N = 12$ and $f_{\text{sw}} = 10\,\text{kHz}$ this would be a bandwidth of $\text{BW} = 480\,\text{kHz}$. In case higher-order harmonics are required to operate with "critical" duty cycle combinations as discussed in **Section III-C**, up to twice that bandwidth would be needed.

In practice, there are parasitic elements L_{par} and R_{par} due to the interconnections of the distributed dc-link capacitors, as indicated in **Fig. 6**. These parasitics, if the dc-link capacitor banks are not carefully designed, might lead to oscillations between the dc-link capacitors of the different phases. This will adversely impact the current balancing control, as parasitic circulating currents are not considered in the derivation of the Fourier series in equation (5). For the considered system with $N = 12$ full-bridge phase modules, simulations indicate that parasitics in the order of $L_{\text{par}} \approx 10\,\text{nH}$ and $R_{\text{par}} \approx 200\,\mu\Omega$ (randomly distributed among the phase modules) do not impact the current balancing performance noticeably.

C. Phase Inductance Mismatch Estimation

The proposed phase current balancing method from **Section III-A** assumes equal phase inductances $L_{\text{i}}^+ = L_{\text{i}}^-$ for all phases in the derivation of the expressions for the current imbalance information $\Delta\underline{A}$. Whereas small inductance variations in the order of $\pm 10\%$ do not noticeably impair the performance of the corresponding balancing controller implementation based on equation (11), larger variations of up to, e.g., $\pm 30\%$ must be expected in certain applications. Then, to still achieve appropriate phase current balancing performance, the effect of phase inductance mismatches on equation (5) should be taken into account.

The inductance variations are in general unknown and an a priori measurement (or calibration) is often not feasible because of costs and possibly changing conditions during the lifetime due to aging effects. However, whereas the ac components of the dc-link capacitor current are mostly defined by the *average* phase current and the switching states of the bridge-legs, the ac components of the output capacitor result only from the ac (ripple) components of the phase currents, i.e., change with the individual inductance values. Advantageously, therefore, a similar approach as for estimating the phase current imbalance (see **Section III-A**) can be used to estimate the relative inductance variations during converter operation by means of a single (indirect, again via the $\mathrm{d}v/\mathrm{d}t$) measurement of the *output* capacitor current with a sensing circuit like in **Fig. 6**.[5] Again, the harmonic spectrum is utilized to estimate the phase inductance variations: The vector $\widetilde{\underline{L}} = [\frac{1}{L_1^+},\ \frac{1}{L_1^-},\ \frac{1}{L_1^+},\ \frac{1}{L_1^-},\ \ldots]^T$ containing the phase inductance mismatch information can be determined by considering the complex-valued Fourier coefficients for the output capacitor current waveform and applying similar transformations as in equation (6), i.e.,

$$\begin{aligned}\widetilde{\underline{L}} &= \underline{\underline{S}}_{2\text{N}}{}^{-1} \cdot \underline{\underline{P}}_{\text{L}}{}^{-1} \cdot \underline{c}_{\text{meas,V}_{\text{out}}} \\ &= \underline{\underline{S}}_{2\text{N}}{}^{-1} \cdot \underline{\underline{P}}_{\text{L}}{}^{-1} \cdot (\widetilde{\underline{\underline{S}}}_{4\text{N}} \cdot \underline{v}_{\text{meas,V}_{\text{out}}}),\end{aligned} \tag{17}$$

where $\underline{\underline{P}}_{\text{L}}$ is again a (2×2) block-diagonal matrix and $\underline{\underline{S}}_{2\text{N}}$ is the $2N$-point DFT matrix; note the similarity to (8). This information can subsequently be used to compute a refined phase current unbalance estimate by including the effect of inductance variations as $\Delta\underline{A} = \Delta\underline{A}_{\text{iCin}} + \Delta\underline{A}_{\text{L}}$ in (11):

$$\Delta\underline{A} = \underline{\underline{\text{Left}}} \cdot \underline{\underline{P}}_{\text{D}}{}^{-1} \cdot (\widetilde{\underline{\underline{S}}}_{4\text{N}} \cdot \underline{v}_{\text{meas}} - \underline{\underline{C}}_{\text{L}} \cdot \underline{\underline{S}}_{2\text{N}} \cdot \widetilde{\underline{L}}). \tag{18}$$

There, $\underline{\underline{C}}_{\text{L}}$ represents a (2×2) block-diagonal matrix that is used to obtain the correction terms $\Delta\underline{A}_{\text{L}}$. A more detailed description is beyond the scope of this paper and will be addressed in future work.

D. Carrier-to-Phase Re-Ordering

As observed in **Fig. 5b**, the output voltage exhibits an increased ripple after the balancing controller becomes active, because of

[5]Note that the output capacitor is typically smaller in size compared to the dc-link capacitor, and can be centrally placed in contrast to the practically required distributed placement of the input dc-link capacitor bank to keep the commutation loops as small as possible.

the according minor modifications of the individual bridge-leg duty cycles. One approach to mitigate this increased ripple consists in modifying the intra-branch interleaving angles ϕ_{intra} as in [11], [12]. For example, in [12], the case of non-ideal ripple cancellation due to inductance tolerances is considered and a suitable rearranging of the carrier-to-phase assignment is proposed such that phases with similar peak-to-peak ripple amplitudes operate with $180°$ phase shift; this reduces the measured voltage ripple by up to 45%. However, the approach is limited to the effect of inductance variations only, requires a current sensor, and a dedicated calibration switching sequence to determine an improved carrier-to-phase assignment.

In the case at hand, an increased output voltage ripple can as well arise from phase inductance tolerances, but in particular also due to the adjustment of the individual bridge-leg duty cycles by the proposed current balancing controller. Here, an improved carrier-to-phase assignment at either the intra-branch or even the inter-branch[6] level resulting in better ripple cancellation can be found based on the current balancing controller outputs $\Delta\underline{D}^+$ and $\Delta\underline{D}^-$ from **Fig. 4** and, possibly, also based on the phase inductance estimation (see **Section IV-C**). Advantageously, no further sensors or additional calibration procedures are needed. In the most fundamental case of only using the current balancing controller outputs $\Delta\underline{D}^+$ and $\Delta\underline{D}^-$ and restricting the re-ordering to only the intra-branch level by simply assigning the carriers according to the duty cycle values, already a reduction of the output voltage ripple by around 44% is achieved, see **Fig. 7**.

V. Conclusion

In certain applications of multi-phase full-bridge dc-dc converters, losses (e.g., for operation inside of cryostats when supplying HTS magnets as considered here) and/or costs prevent the use of per-phase current sensors that are otherwise employed to ensure balanced phase currents. Therefore, this paper introduces a new phase current balancing control method based on indirectly sensing the dc input capacitor current via the $\mathrm{d}v/\mathrm{d}t$ and using the known switching states of the converter phases. Detailed mathematical derivations lead to a computationally efficient frequency-domain processing method. Further, for very small output voltages (as, e.g., for the considered application with HTS magnet loads) the computations can be simplified. Both cases are verified by detailed circuit simulations of a system with 12 full-bridge phase modules. Practical aspects such as the realization of the dc input capacitor sensing circuitry for cases with the dc-link capacitor distributed among the phase modules are discussed. Finally, the current balancing control can be improved by means of an additional phase inductance mismatch estimation based on indirectly sensing the output capacitor current, and the output voltage ripple can be decreased by employing a low-effort carrier-to-phase re-assignment based on the balancing

[6]The intra-branch level implementation does not consider the mutual cancellation of the output current ripples from the two branches, whereas this superposition would be included in an inter-branch level consideration.

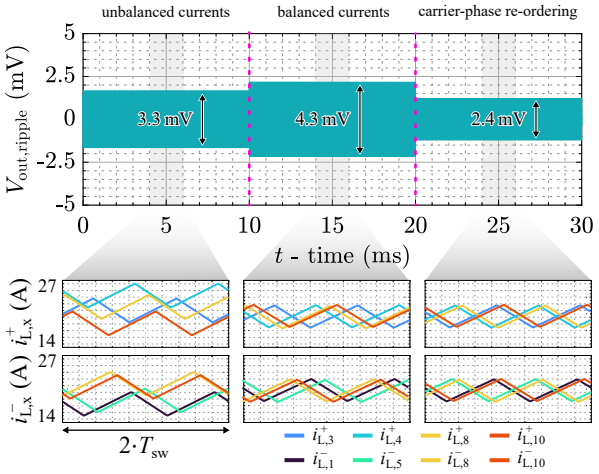

Fig. 7. Carrier-to-phase re-ordering on the intra-branch level utilizing the duty cycle adjustments from the current balancing controller. The simulation results show the output voltage ripple (ac coupling) at the top and zoomed views of four (out of $N = 12$) exemplary phase currents of the $\oplus$- and the $\ominus$-branch.

controller outputs; these aspects will be analyzed in more detail in the scope of future work.

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