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Novel Bidirectional Single-Stage Isolated 600-V GaN M-BDS-Based Single-/Three-Phase-Operable EV On-Board Charger

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Abstract

Next generation On-Board Chargers (OBCs) should comprise only a single high-frequency-isolated ac-dc converter stage that realizes bidirectional power flow from not only a three-phase but also a single-phase grid to the Electric Vehicle (EV) battery and should cover a wide input-output voltage range. This paper introduces the novel isolated Y-Rectifier with series-resonant operation (iYR$_S$), which utilizes 600 V GaN Monolithic Bidirectional Switches (M-BDSs) and complies with the aforementioned requirements for next-generation OBCs. The operating principles and control methods for buck-boost operation from a three-phase and a single-phase mains with the same rated power are detailed and validated by circuit simulations. The voltage and current stresses of the main power components are derived, and a 6.6 kW design example indicates expected efficiencies of almost 97% for three-phase and 97.5% for single-phase operation.

1 Introduction

Electric Vehicle (EV) On-Board Chargers (OBCs) face very demanding requirements including galvanic isolation between the grid and the EV battery, a wide battery voltage range, nominal-power operation from three-phase and single-phase grids, high power density, and bidirectional power flow [1]. The state-of-the-art approach for OBCs is a two-stage system comprising of a power-factor-correction (PFC) rectifier front-end followed by an isolated dc-dc converter stage [2], which, however, is disadvantageous as the power is converted twice, and two converter stages need to be designed and built. High-frequency-(HF)-isolated single-stage ac-dc converters with either a Dual Active Bridge (DAB) [3], [4] or Series-Resonant (SR) operating mode [5] are thus an attractive alternative to meet OBC requirements. So far, however, the extensive research into single-stage isolated three-phase PFC ac-dc converters [3]–[22] has not yet considered single-phase operation, or only with a limited output power [23]. This shortcoming is addressed by

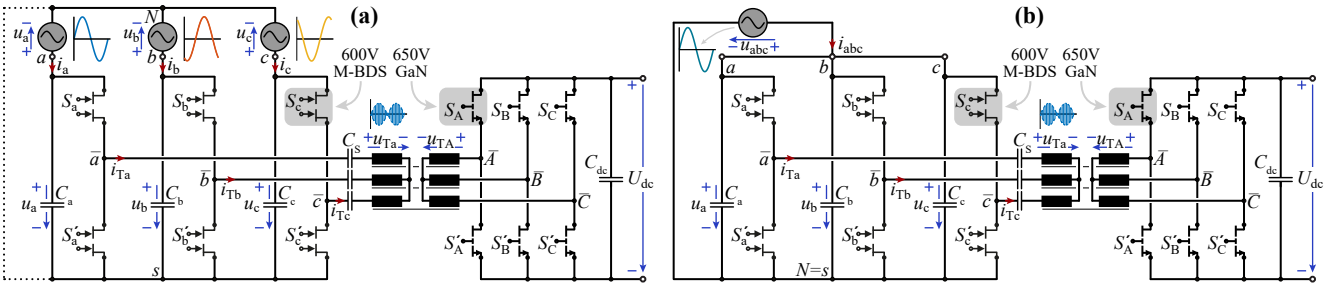

Fig. 1: The proposed topology of the isolated Y-Rectifier with series resonant operation (iYR$_S$) utilizing 600 V GaN M-BDSs in the ac-front-end to directly interface with the **(a)** three-phase (325 V$_{peak}$ line-to-neutral; 400 V line-to-line rms) and **(b)** single-phase (325 V$_{peak}$ line-to-neutral) grid. By employing a novel resonant modulation, bidirectional charging at nominal power is achieved with both configurations.

Tab. 1: Considered system specifications.

Parameter	Symbol	Value	Unit
Grid Voltage[1]	3ϕ, $u_{\mathrm{a,b,c}}$	230	V_{rms}
	1ϕ, u_{abc}	230	V_{rms}
Grid Freq.	f_{ac}	50	Hz
Switching Freq.	f_{sw}	72	kHz
Rated Output Power	P_{dc}	6.6	kW
Output Voltage	U_{dc}	250-450	V

[1]line-to-neutral

the new bidirectional isolated Y-Rectifier topology[1] with a SR operating mode (iYR$_S$) as depicted in **Fig. 1**. The iYR$_S$ ac-front-end employs novel GaN-based Monolithic Bidirectional Switches (M-BDSs): with the ac-front-end M-BDSs blocking voltages defined by the grid peak line-to-neutral voltage, 600 V rated semiconductors can be used for interfacing the European 400 V (line-to-line rms) grid. The SR modulation enables full soft switching in the ac-front-end in both single- and three-phase operation for a significant share of the desired output voltage range $U_{\mathrm{dc}} \in [250\,\mathrm{V}, 450\,\mathrm{V}]$.

In the following, first **Section 2** explains the operating method of the iYR$_S$ for three- and single-phase buck-boost operation via space vector (SV) diagrams and simulation results. Given the specifications in **Tab. 1**, **Section 3** then provides basic design considerations along with key component stresses and provides an efficiency estimate of an exemplary iYR$_S$ design. Finally, **Section 4** concludes the paper.

2 Operating Method

The method of operation of the iYR$_S$ topology is provided in this section for both, the three-phase and single-phase operation with the use of SV diagrams and circuit simulations. First, only boost operation is considered, and then the concept is extended to a buck-boost operation to enable a wide output voltage range.

2.1 Three-Phase

In the three-phase configuration (**Fig. 1a**), the ac-front-end semiconductors are switched synchronously with a duty cycle d_{abc} = 50% and translate the grid input voltages u_{a}, u_{b}, u_{c} into an amplitude-modulated HF three-phase transformer voltage system u_{Ta}, u_{Tb}, u_{Tc} [22] as can be observed from the simulation results in (**Fig. 2a.i**). Here, the series capacitor C_{S} forms a resonant tank with the transformer inductance L_{S} in each phase, which is tuned to the switching frequency f_{sw} similar to a SR dc-dc converter [25].[2] In addition, the series capacitors C_{S} block half the instantaneous phase voltage and thus only the HF component varying between $\pm\frac{1}{2}u_{\mathrm{a}}$, $\pm\frac{1}{2}u_{\mathrm{b}}$, $\pm\frac{1}{2}u_{\mathrm{c}}$ acts on the primary side of the resonant tank (a zoom-in on the waveforms is presented in **Fig. 2a.ii**). A SV representation of the primary-side transformer voltages ($\underline{u}_{\mathrm{Tabc}}$) is presented in **Fig. 2b** and the two synchronous switching transitions of the primary-side stage, α and β (see u_{Ta} in **Fig. 2a.ii**), result in the primary-side SV $\underline{u}_{\mathrm{Tabc}}$ in **Fig. 2b** toggling between $\pm\frac{1}{2}$ of the three-phase grid voltage SV $\underline{u}_{\mathrm{a,b,c}}$. The dc-stage generates a secondary-side transformer voltage SV $\underline{u}_{\mathrm{TABC}}$ (displayed in **Fig. 2b** for a unity transformer turns ratio) which is in phase with the primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$ during the first Ⅰ and second Ⅱ half switching period $\frac{1}{2}T_{\mathrm{sw}} = 1/(2f_{\mathrm{sw}})$ and shows approximately equal amplitude,[3] resulting in naturally sinusoidal low-frequency (LF) grid currents $\bar{i}_{\mathrm{a}}$, $\bar{i}_{\mathrm{b}}$, $\bar{i}_{\mathrm{c}}$. Note that the resonant tanks show approximately zero impedance at the switching frequency and thus the power flow can be adjusted by slightly adjusting the magnitude of the dc-stage voltage SV $|\underline{u}_{\mathrm{TABC}}|$ similar to a SR dc-dc converter [25]: If, e.g., $|\underline{u}_{\mathrm{TABC}}|$ is selected slightly smaller than $|\underline{u}_{\mathrm{Tabc}}|$ the resulting voltage difference ΔU is applied to the resonant tanks which are energized, resulting in an increase in the three-phase power transfer and ultimately to an increase in the output voltage.

The operation of the dc-stage can be controlled by means of a simple Pulse Width Modulation (PWM) strategy with two duty cycles which are, e.g., for

[1]Note that the main power circuit structure is identical to [22]. However, here a resonant operating mode is employed.

[2]In contrast, in [22] the series capacitor C_{S} is sized to show negligible impedance compared to the transformer inductance L_{S} at the switching frequency to enable a DAB-type modulation.

[3]In the time domain this corresponds to the dc-stage generating HF differential-mode voltages $u_{\mathrm{TA}}, u_{\mathrm{TB}}, u_{\mathrm{TC}}$ recreating the voltage-time area of the primary-side transformer voltages $u_{\mathrm{Ta}}, u_{\mathrm{Tb}}, u_{\mathrm{Tc}}$ within each $\frac{1}{2}T_{\mathrm{sw}}$ period as illustrated in **Fig. 2a.ii**.

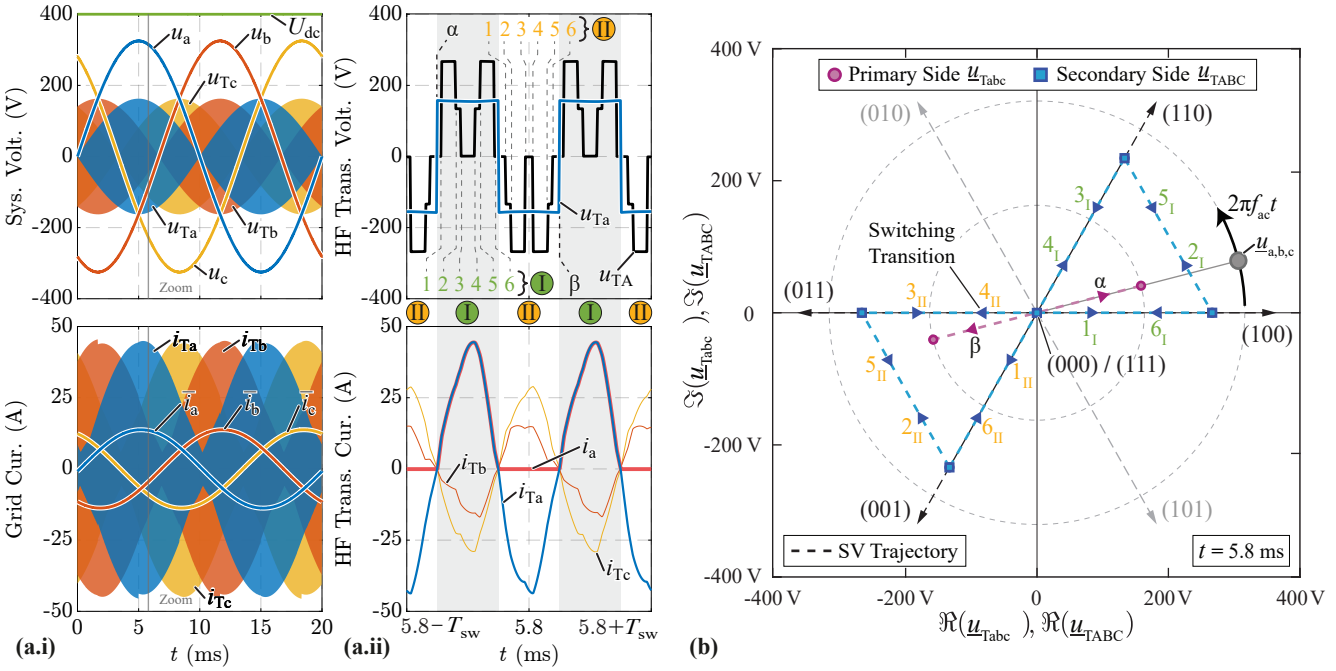

Fig. 2: (a) Simulated key voltage and current waveforms (generated using PLECS [24]) of the proposed iYR$_S$ topology shown in **Fig. 1a** for three-phase PFC operation over a mains period **(a.i)** and over two switching periods T_{sw} around t = 5.8 ms **(a.ii)** . **(b)** Space vector (SV) representation of the HF voltage waveforms in **(a.ii)**. The ac-front-end operation with d_{abc} = 50% results in a primary-side transformer voltage SV $\underline{u}_{\mathrm{Tabc}}$ with half the magnitude of the grid voltage SV $\underline{u}_{\mathrm{a,b,c}}$ and toggling between in-phase and anti-phase orientation in every half switching period (the primary-side switching transitions are labelled with α and β). The dc-stage generates a secondary-side voltage SV $\underline{u}_{\mathrm{TABC}}$ recreating $\underline{u}_{\mathrm{Tabc}}$ during the first Ⓘ and second Ⓘⓘ $\frac{1}{2}T_{sw}$ period (the dc-stage switching transitions are numbered with 1...6). Simulation parameters: $u_{\mathrm{a,b,c}}$ = 230 V (rms; line-neutral), f_{sw} = 72 kHz, L_S = 30 µH, C_S = 163 nF, U_{dc} = 400 V, P_{dc} = 6.6 kW.

phase a defined as

$$d_{\mathrm{A,I}}(t) = \min\left(\frac{\Delta U + \hat{u}_{\mathrm{a,b,c}}}{U_{dc}}\frac{N_2}{N_1}, 1\right)\frac{u_a(t)}{2\hat{u}_{\mathrm{a,b,c}}} + \frac{1}{2} \quad (1)$$

for the first Ⓘ and $d_{\mathrm{A,II}} = 1 - d_{\mathrm{A,I}}$ for the second Ⓘⓘ $\frac{1}{2}T_{sw}$ period, with $d_{\mathrm{A,I}}, d_{\mathrm{A,II}} \in [0,1]$. Note that $\Delta U \ll \hat{u}_{\mathrm{a,b,c}}$ allows to adjust the magnitude of the secondary-side voltage SV $|\underline{u}_{\mathrm{TABC}}|$ to regulate the power flow. The switching signals are easily realised with a synchronised secondary-side carrier with $2f_{sw}$ (i.e., double the switching frequency of the ac-front-end) which is compared to $d_{\mathrm{A,I}}$ and $d_{\mathrm{A,II}}$ in alternation during the first and the second $\frac{1}{2}T_{sw}$ period, respectively. The resulting secondary-side voltage SV $\underline{u}_{\mathrm{TABC}}$ trajectory[4] is presented in **Fig. 2b** with the sequence of switching states

$$(000)\underset{1_{\mathrm{I}}}{\blacktriangleright}(100)\underset{2_{\mathrm{I}}}{\blacktriangleright}(110)\underset{3_{\mathrm{I}}}{\blacktriangleright}(111)\underset{4_{\mathrm{I}}}{\blacktriangleright}(110)\underset{5_{\mathrm{I}}}{\blacktriangleright}(100)\underset{6_{\mathrm{I}}}{\blacktriangleright}(000), \quad (2)$$

in the first $\frac{1}{2}T_{sw}$ period Ⓘ. Similarly, for the second $\frac{1}{2}T_{sw}$ period Ⓘⓘ the generated switching sequence is

$$(000)\underset{1_{\mathrm{II}}}{\blacktriangleright}(001)\underset{2_{\mathrm{II}}}{\blacktriangleright}(011)\underset{3_{\mathrm{II}}}{\blacktriangleright}(111)\underset{4_{\mathrm{II}}}{\blacktriangleright}(011)\underset{5_{\mathrm{II}}}{\blacktriangleright}(001)\underset{6_{\mathrm{II}}}{\blacktriangleright}(000). \quad (3)$$

The corresponding secondary-side time-domain voltage of phase a, u_{TA}, is shown in **Fig. 2a.ii**, which is in phase with the primary-side voltage u_{Ta} (i.e., in contrast to a DAB-type modulation, no HF phase shift is introduced in between u_{Ta} and u_{TA}) and shows an identical $\frac{1}{2}T_{sw}$ period average value, such that quasi-sinusoidal resonant tank currents i_{Ta}, i_{Tb}, i_{Tc} result.

To achieve symmetrical stresses of the dc-stage high- and low-side power transistors, the secondary-side carrier is flipped (i.e., phase shifted by 180°) for each 60° sector. Note that, alternatively, the dc-stage could be modulated with the SV modulation from [19] which enables to lower the (average) switching frequency from $2f_{sw}$ to $\frac{4}{3}f_{sw}$.

[4]Note that the transitions in **Fig. 2b** and **Fig. 3b** are highlighted just for illustration purposes: The voltage SVs $\underline{u}_{\mathrm{Tabc}}$ and $\underline{u}_{\mathrm{TABC}}$ are defined by corresponding discrete endpoints in the complex plane (corners and midpoint of a hexagon) and the transition from one space vector to the following happens instantaneously.

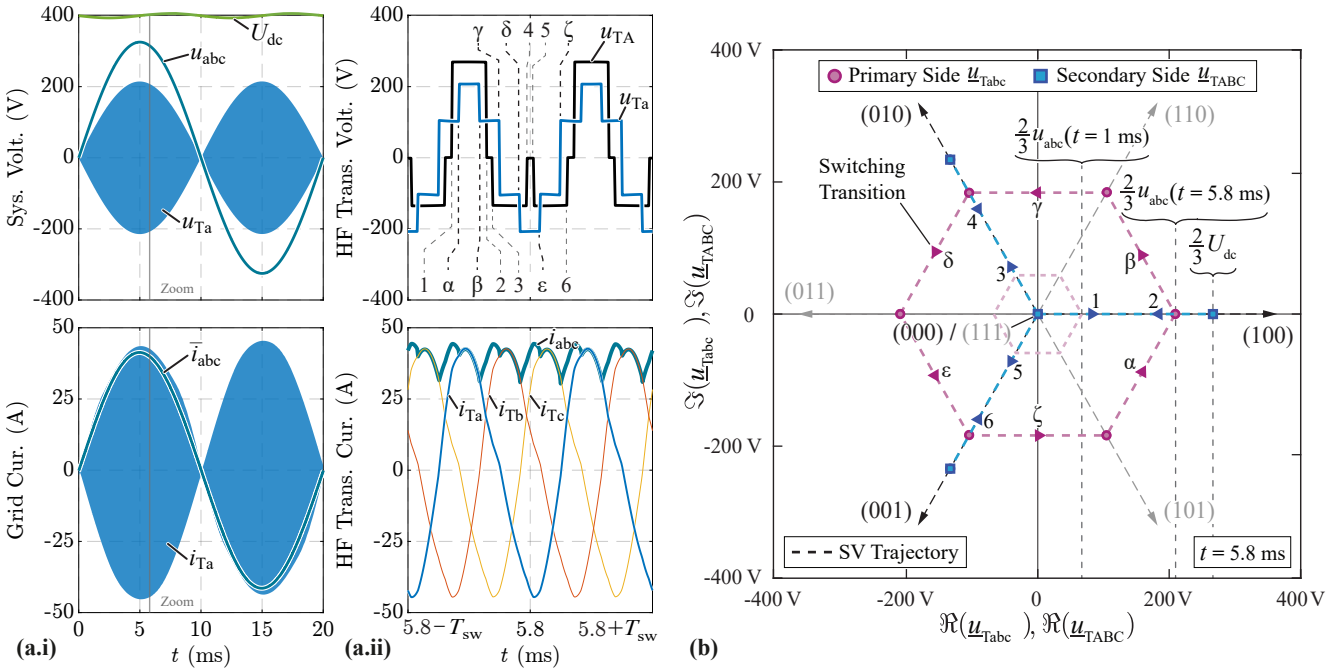

Fig. 3: (a) Simulated key waveforms (generated using PLECS [24]) of the proposed iYR$_S$ topology shown in **Fig. 1b** for single-phase PFC operation over a mains period **(a.i)** and over two switching periods T_{sw} around t = 5.8 ms **(a.ii)**. **(b)** Space vector (SV) representation of the HF voltage waveforms in **(a.ii)**. In single-phase operation, both, the primary- and the secondary-side half-bridges operate with 120° PWM carrier phase shift, resulting in a hexagonal trajectory of the primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$ in **(b)**. Note that the amplitude of the active primary-side voltage SV is proportional to the instantaneous grid voltage $u_{\mathrm{abc}}(t)$ (i.e., the size of the hexagon changes with the grid voltage). The primary-side and secondary-side switching transitions are labelled with α ... ζ and 1 ... 6, respectively. Simulation parameters: u_{abc} = 230 V$_{\mathrm{rms}}$, f_{sw} = 72 kHz, L_S = 30 µH, C_S = 163 nF, U_{dc} = 400 V, P_{dc} = 6.6 kW.

2.2 Single-Phase

For single-phase operation (**Fig. 1b**), the ac-front-end half-bridges are parallel-connected to the grid line and neutral terminals and operate with d_{abc} = 50% and a 120° PWM carrier phase shift, thereby translating the single-phase grid voltage u_{abc} into a symmetric HF three-phase voltage system u_{Ta}, u_{Tb}, u_{Tc}. Thus, the operation resembles that of a multi-phase SR dc-dc converter, where the (bipolar) input voltage is varying with the grid input voltage u_{abc} as indicated in **Fig. 3a**. **Fig. 3b** presents the SV representation of the transformer voltages, and the aforementioned 120° PWM carrier phase shift of the ac-front half-bridges results in a hexagonal trajectory of the primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$. Note that the instantaneous voltage SV magnitude $|\underline{u}_{\mathrm{Tabc}}| = \frac{2}{3}u_{\mathrm{abc}}$ is proportional to the instantaneous grid voltage value and thus the area of the primary-side voltage SV hexagon changes over time with twice the grid frequency $2f_{\mathrm{ac}}$ and the time-domain transformer voltages u_{Ta}, u_{Tb}, u_{Tc} (see **Fig. 3a.i**) are amplitude modulated by the single-phase grid voltage u_{abc}. Note that in contrast to three-phase operation, here the series capacitors C_S do not block any LF voltage components.

Similarly, the secondary side half-bridges operate at f_{sw} (i.e., the same switching frequency as the ac-front-end) with a 120° PWM carrier phase shift and identical duty cycles $d_A = d_B = d_C$ and

$$d_A = \frac{1}{\pi}\arcsin\left(\min\left(\frac{|u_{\mathrm{abc}}(t)| + \Delta U}{U_{\mathrm{dc}}\frac{N_1}{N_2}}, 1\right)\right), \quad (4)$$

utilizing again the small voltage difference ΔU to regulate the power flow. During, e.g., the positive mains period, and for a duty cycle $d_A = d_B = d_C <$ 1/3 (i.e., $|u_{\mathrm{abc}}| < \frac{N_1}{N_2}U_{\mathrm{dc}}$ for ΔU = 0), the sequence of switching states is

$$(000)\underset{1}{\blacktriangleright}(100)\underset{2}{\blacktriangleright}(000)\underset{3}{\blacktriangleright}(010)\underset{4}{\blacktriangleright}(000)\underset{5}{\blacktriangleright}(001)\underset{6}{\blacktriangleright}(000), \quad (5)$$

as indicated for the voltage SV $\underline{u}_{\mathrm{TABC}}$ in **Fig. 3b** (utilized dc-stage switching states are labelled in black; non-utilized switching states in gray). In contrast, for 1/3 < $d_A = d_B = d_C <$ 1/2 the secondary SV trajectory changes to a hexagonal shape with the

sequence of switching states

$$(101)\blacktriangleright(100)\blacktriangleright(110)\blacktriangleright(010)\blacktriangleright(011)\blacktriangleright(001)\blacktriangleright(101) \quad (6)$$

resulting in a counterclockwise sequence similar to the primary-side SV trajectory $\underline{u}_{\mathrm{Tabc}}$.
Note that, as the grid voltages becomes negative, the dc-stage switching signals generated according to **Eq. (5)** need to be inverted resulting, e.g., for phase a, in an effective conduction time of the high-side power transistor

$$d'_{\mathrm{A}} = \begin{cases} d_{\mathrm{A}}, & u_{\mathrm{abc}}(t) \geq 0 \\ 1 - d_{\mathrm{A}}, & u_{\mathrm{abc}}(t) < 0, \end{cases} \quad (7)$$

which advantageously facilitates equal power transistor current stresses of the top and bottom dc-stage power transistors.

2.3 Buck-Boost Operation

The presented three- and single-phase modulation concepts rely on controlling the power flow by adjusting the amplitude of the voltage SV $|\underline{u}_{\mathrm{TABC}}|$ generated by the dc-stage by a small ΔU. This, however, imposes a voltage limit $\frac{N_1}{N_2}U_{\mathrm{dc}} > \hat{u}_{\mathrm{a,b,c}}$ and limits the iYR$_{\mathrm{S}}$ topology to boost operation, which is incompatible with the desired dc output ranges stated in **Tab. 1**. This limitation is resolved by additionally adjusting the ac-front-end modulation to maintain power flow control in buck operation with $\frac{N_1}{N_2}U_{\mathrm{dc}} < \hat{u}_{\mathrm{a,b,c}}$.

For three-phase operation, the ac-front-end duty cycle can then be defined as

$$d_{\mathrm{abc}} = \frac{1}{\pi}\arcsin\left(\min\left(\frac{U_{\mathrm{dc}}\frac{N_1}{N_2} - \Delta U}{\hat{u}_{\mathrm{a,b,c}}}, 1\right)\right), \quad (8)$$

such that the ac-front-end takes over the power flow control in buck mode. Therefore, d_{abc} deviates from 50% only when $\frac{N_1}{N_2}U_{\mathrm{dc}} < \hat{u}_{\mathrm{a,b,c}}$ (for $\Delta U = 0$).
The ΔU-based power flow control defined with **Eq. (1)** and **Eq. (8)** automatically results in either the ac-front-end (boost) or the dc-stage (buck) operating in saturation with the maximum SV voltage amplitude, while the other stage assures power flow controllability. This enables the desired wide output voltage range operation and **Fig. 4a** shows simulation results where the iYR$_{\mathrm{S}}$ supplies an electronic dc load which sweeps the output

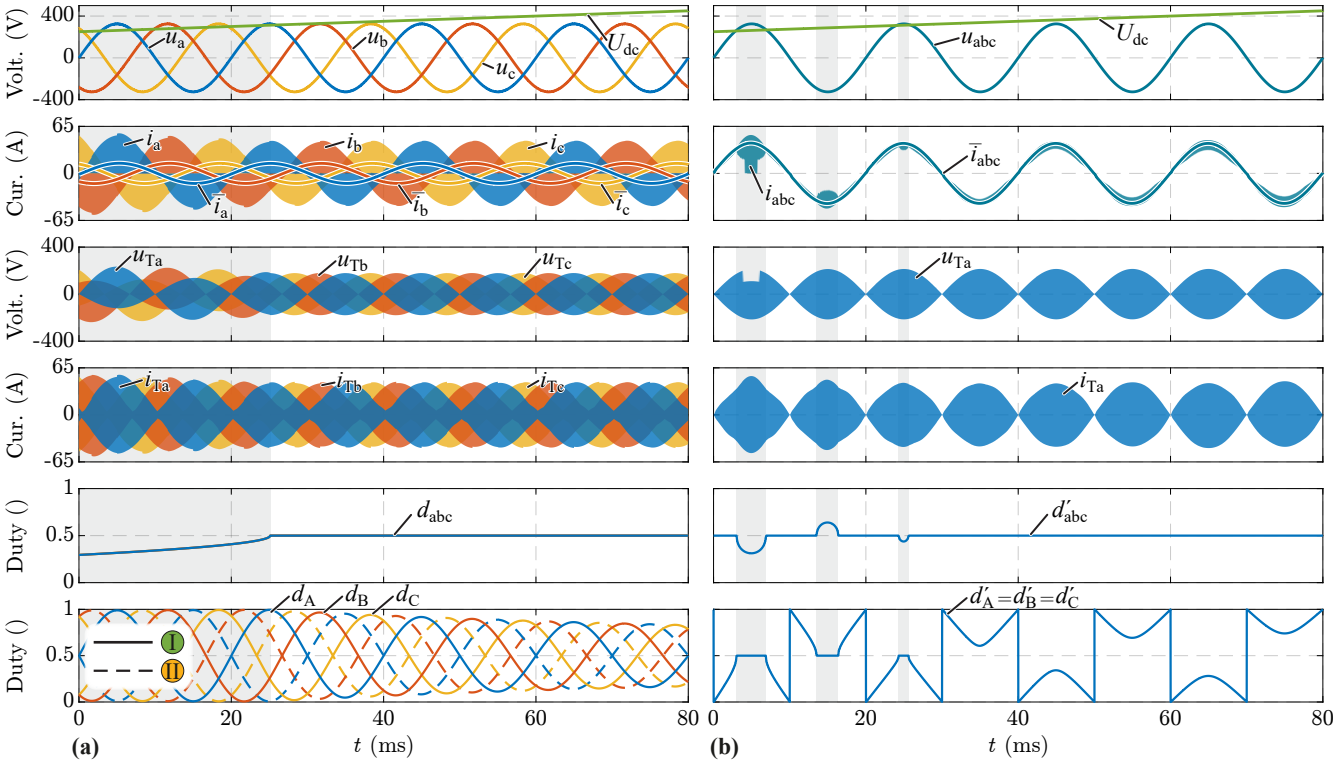

Fig. 4: Simulation waveforms (generated using PLECS [24]) showing the transition from buck (grey background) to boost operation of the iYR$_{\mathrm{S}}$ for a dc output voltage ramp from 250 V to 450 V for **(a)** three-phase and **(b)** single-phase operation. The secondary side is connected to an electronic load defining the dc voltage, and the iYR$_{\mathrm{S}}$ control maintains a constant power transfer of 6.6 kW.

voltage from 250 V to 450 V and the iYR$_S$ control ensures a continuous power transfer of P_{dc} = 6.6 kW when transitioning from buck (highlighted in grey) to boost operation.

In contrast, for single-phase operation the modulation is adjusted based on the instantaneous absolute grid voltage value $|u_{abc}(t)|$ (instead of the grid voltage amplitude as in three-phase operation), i.e.,

$$d_{abc} = \frac{1}{\pi} \arcsin\left(\min\left(\frac{U_{dc}\frac{N_1}{N_2} - \Delta U}{|u_{abc}(t)|}, 1 \right) \right). \quad (9)$$

To realize equal conduction stresses for the high- and low-side M-BDSs over a mains period, the ac-front-end duty cycle is deviated symmetrically to values below and above 0.5 for the positive and negative grid interval, respectively, with

$$d'_{abc} = \begin{cases} d_{abc}, & u_{abc}(t) \geq 0 \\ 1 - d_{abc}, & u_{abc}(t) < 0. \end{cases} \quad (10)$$

Fig. 4b presents simulation results for single-phase operation, and a dynamic transition between buck (shaded grey areas) and boost operation can be observed. Note that the ac-front-end and dc-stage duty cycles deviate from 50% only in buck and boost operation, respectively.

3 Design and Performance Estimation

To provide a first performance evaluation of the iYR$_S$, a basic design example for a 6.6 kW converter according to **Tab. 1** is conducted (the resulting converter parameters are listed in **Tab. 2**) and the component stresses and losses are provided.

3.1 Component Selection

The dc-stage power transistors are subject to voltages up to U_{dc} = 450 V (not considering switching overvoltages) and can thus be realized with 650-V-rated GaN Systems GS-065-060-5-T-A which feature a low on-state resistance of 25 mΩ (typ.). The PLECS [24] thermal model (provided by the manufacturer) is used to assess the conduction and switching losses presented in **Tab. 3**, where further a thermal interface material (TIM) with a thermal impedance of 52 K mm^2/W [26] is considered to interface the device case and a water-cooled cold plate with a (maximum) temperature of 60 °C.
The M-BDSs of the ac-front-end are blocking voltages of up to $\hat{U}_{abc}$ = 325 V, and can thus be realized with 600 V/650 V GaN technology. The switching and conduction losses are estimated by assuming a virtual M-BDS version of the GS-065-060-5-T-A which has the same switching- and conduction-loss characteristics as the unipolar GaN device considered for the dc-stage.[5]
A transformer, with turns ratio $N_1 : N_2$ = 1:1 and a leakage inductance of L_S = 30 µH is considered. For brevity, the transformer losses (P_{T_a}) at rated power are obtained by assuming a typical efficiency of η_T = 99.5 %. The series capacitance C_S = 163 nF is selected such that the desired resonant tank frequency $f_0 = f_{sw}$ is achieved. The input capacitors C_a = 2.5 µF are selected such that a 2% reactive input current limit at nominal power operation is ensured. The dc output capacitance C_{dc} = 4.2 mF is sized for single-phase operation such that the maximum allowable peak-to-peak output voltage ripple ΔU_{dc} = 20 V is not exceeded at the worst-case operating point with U_{dc} = 250 V and nominal power delivery P_{dc} = 6.6 kW. Note that a more compact system realization could be achieved by employing an active power pulsation buffer concept [27]–[29]. Assuming the use of capacitors with a high-quality dielectric material with a low dissipation factor, the filter, dc and series capacitor losses are neglected here.

Tab. 2: Considered converter parameters.

Description	Identifier	Value	Unit
Input Cap.	C_a	2.5	µF
M-BDS[1]	S_a,S'_a	25 650	mΩ$_{typ}$ V
Series Cap.	C_S	163	nF
Leakage Ind.	L_S	30	µH
Turns Ratio	$N_1 : N_2$	1:1	
DC Side Semi.[1]	S_A,S'_A	25 650	mΩ$_{typ}$ V
DC Cap.	C_{dc}	4.2	mF

[1] GaN Systems GS-065-060-5-T-A (a virtual M-BDS version is assumed for the ac-front-end)

[5] Note that such an M-BDS device does currently not exist. However, current R&D activities in the field of GaN M-BDS make it very likely that such a low on-resistance M-BDS device will be available in a next-generation product.

Tab. 3: Component stresses and loss evaluation for the converter in **Fig. 1** at a nominal output power of 6.6 kW and an output voltage of 400 V.

Parameter	3-Phase	1-Phase	Unit
$\hat{i}_{\mathrm{T_a}}$	45.4	45.3	A
$I_{\mathrm{T_a}}$	21.8	21.8	$\mathrm{A_{rms}}$
$I_{\mathrm{S_a}} = I_{\mathrm{S'_a}}$ [1]	15.4	15.4	$\mathrm{A_{rms}}$
$I_{\mathrm{S_A}} = I_{\mathrm{S'_A}}$	15.4	15.6	$\mathrm{A_{rms}}$
$P_{\mathrm{S_a,Cond}} = P_{\mathrm{S'_a,Cond}}$ [1]	9.0	9.0	W
$P_{\mathrm{S_a,Sw}} = P_{\mathrm{S'_a,Sw}}$ [1]	0.9	0.7	W
$P_{\mathrm{T_a}}$	11	11	W
$P_{\mathrm{S_A,Cond}} = P_{\mathrm{S'_A,Cond}}$	10.2	9.7	W
$P_{\mathrm{S_A,Sw}} = P_{\mathrm{S'_A,Sw}}$	9.9	4.6	W
P_{Total}	213	177	W
η	96.9	97.4	%

[1] Note that unequal power transistor stresses result in three-phase buck operation.

3.2 Component Stresses and Performance

The component stresses, and primary loss sources of the converter design from **Section 3.1** are evaluated using PLECS [24] simulations considering nominal power operation with U_{dc} = 400 V for both, three and single-phase operation with the results listed in **Tab. 3**. The predominantly soft-switching operation of the ac-front-end M-BDSs results in low switching losses ($P_{\mathrm{S_a,Sw}} = P_{\mathrm{S'_a,Sw}}$) for both, single- and three-phase operation, but is only possible for pure boost operating regions of the $\mathrm{iYR_S}$.[6] It can be observed that the single-phase operation with a calculated efficiency of η = 97.4 % is superior to the three-phase operation with η = 96.9 %. The main reason for this performance deviation are the dc-side semiconductor hard-switching losses, which are elevated in three-phase operation due to the operation with twice the ac-front-end switching frequency $2f_{\mathrm{sw}}$ discussed earlier. As mentioned, the dc-stage could also be modulated according to [19] to lower the (average) switching frequency to $\frac{4}{3}f_{\mathrm{sw}}$ which promises efficiency gains.

[6] Note that hard-switching transitions will occur when operating in buck mode; E.g. for nominal power operation with an output voltage U_{dc} = 250 V the calculated efficiency drops to η = 95.8 % in three-phase and η = 97.2 % in single-phase operation.

4 Conclusion

The requirements of next-generation On-Board Chargers (OBCs) demand compact and lightweight converter realizations that can operate under a broad range of operating conditions. This paper introduces a new isolated Y-rectifier with a series-resonant operation ($\mathrm{iYR_S}$), which utilizes 600 V GaN M-BDSs in the ac-front-end to operate with nominal power in both, a 400 V (line-to-line rms) three-phase and a single-phase grid. The novel series-resonant modulation enables buck-boost operation and bidirectional power flow with fully sinusoidal grid currents and full soft switching of the ac-front-end transistors for a significant proportion of the desired output voltage range; thus, an exemplary 6.6 kW design achieves estimated efficiencies of 96.9% in three-phase and 97.4% in single-phase configuration.

References

[1] H. Wouters and W. Martinez, "Bidirectional on-board chargers for electric vehicles: State-of-the-art and future trends," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 693–716, Jan. 2024.

[2] C. Wei, H. Xie, Y. Liu, Z. Hu, and J. Shao, "A SiC based high efficiency 22kW bi-directional EV on-board charger," in *Proc. Power Convers. Intelligent Motion Conf. (PCIM)*, Nuremberg, Germany, 2021.

[3] D. Menzi, F. Krismer, T. Ohno, J. Huber, J. W. Kolar, and J. Everts, "Novel bidirectional single-stage isolated three-phase buck-boost PFC rectifier system," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, Mar. 2023.

[4] B. R. De Almeida, J. W. M. De Araujo, P. P. Praca, and D. De S. Oliveira, "A single-stage three-phase bidirectional AC/DC converter with high-frequency isolation and PFC," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8298–8307, Oct. 2018.

[5] M. Zhang, H. Zou, Z. Chen, R. Yu, and A. Q. Huang, "A novel single-stage bidirectional isolated three-phase resonant mode AC-DC PFC converter," in *Proc. Energy Convers. Congr. Expo. (ECCE USA)*, Nashville, TN, USA, Oct. 2023, pp. 2222–2229.

[6] K. Ali, R. K. Surapaneni, P. Das, and S. K. Panda, "An SiC-MOSFET-based nine-switch single-stage three-phase AC–DC isolated converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9083–9093, Nov. 2017.

[7] J. Lee, H. Jeong, T.-T. Le, and S. Choi, "Three-phase single-stage bidirectional CCM soft-switching AC–DC converter with minimum switch count," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2052–2062, Feb. 2023.

[8] G. Li, J. Ruan, K. Wang, Y. Deng, X. He, and Y. Wang, "An interleaved three-phase PWM single-stage resonant rectifier with high-frequency isolation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6572–6582, Aug. 2020.

[9] M. J. Heller, F. Krismer, and J. W. Kolar, "EMI filter design for the integrated dual three-phase active bridge (D3AB) PFC rectifier," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14 527–14 546, Dec. 2022.

[10] J. W. Kolar, U. Drofenik, and F. Zach, "Vienna Rectifier II—A novel single-stage high-frequency isolated three-phase PWM rectifier system," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 674–691, Aug. 1999.

[11] M. Silva, N. Hensgens, J. A. Oliver, P. Alou, Ó. García, and J. A. Cobos, "Isolated Swiss-forward three-phase rectifier with resonant reset," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4795–4808, Jul. 2016.

[12] N. D. Weise, K. K. Mohapatra, and N. Mohan, "Universal utility interface for plug-in hybrid electric vehicles with vehicle-to-grid functionality," in *Proc. IEEE PES Gen. Meeting*, Minneapolis, MN, Jul. 2010, pp. 1–8.

[13] J. J. Sandoval, S. Essakiappan, and P. Enjeti, "A bidirectional series resonant matrix converter topology for electric vehicle DC fast charging," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 3109–3116.

[14] M. J. Harrison, "A cyclo-converter and methods of operation," patent WO2008018802A2, Feb. 14, 2008.

[15] Y. Kosesoy, R. Bonten, H. Huisman, and J. Schellekens, "Control of a zero-voltage switching isolated series-resonant power circuit for direct 3-phase AC to DC conversion," in *Proc. Europ. Conf. Power Electron. Appl. (EPE/ECCE Europe)*, Hanover, Germany, Sep. 2022.

[16] Y. Xu, Z. Wang, Y. Shen, Z. Zou, and M. Liserre, "A VSC-based isolated matrix-type AC/DC converter without bidirectional power switches," *IEEE Trans. Ind. Electron.*, vol. 70, no. 12, pp. 12 442–12 452, Dec. 2023.

[17] P. Cortes, J. Huber, M. Silva, and J. W. Kolar, "New modulation and control scheme for phase-modular isolated matrix-type three-phase AC/DC converter," in *Proc. IEEE Ind. Electron. Soc. Conf. (IECON)*, Vienna, Austria, Nov. 2013, pp. 4899–4906.

[18] L. Gu and K. Peng, "A single-stage fault-tolerant three-phase bidirectional AC/DC converter with symmetric high-frequency Y-Delta connected transformers," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9226–9237, Sep. 2020.

[19] R. Baranwal, K. V. Iyer, K. Basu, G. F. Castelino, and N. Mohan, "A reduced switch count single-stage three-phase bidirectional rectifier with high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9520–9541, 2018.

[20] E. Asa, O. C. Onar, V. P. Galigekere, G.-J. Su, and B. Ozpineci, "A novel three-phase Oak Ridge AC/DC converter for wireless EV charger applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Phoenix, AZ, USA, Jun. 2021, pp. 437–443.

[21] J. E. Bosso, M. Llomplat, G. G. Oggier, and G. O. García, "Isolated bidirectional DC-to-three-phase AC converter for integration of renewable energy sources to electric grid," *IET Power Electronics*, vol. 12, no. 8, pp. 2058–2068, 2019.

[22] D. Menzi, J. W. Kolar, H. Sarango, Ó. Luciá, and J. Huber, "New 600 V GaN single-stage isolated bidirectional 400 V input three-phase PFC rectifier," in *Proc. Energy Convers. Congr. Expo. (ECCE USA)*, Nashville, TN, USA, Oct. 2023.

[23] H. Kim, J. Park, S. Kim, R. M. Hakim, H. Belkamel, and S. Choi, "A single-stage electrolytic capacitorless EV charger with single- and three-phase compatibility," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6780–6791, Jun. 2022.

[24] J. Allmeling and W. Hammer, "PLECS-piece-wise linear electrical circuit simulation for Simulink," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst. (PEDS)*, Hong Kong, China, 1999, 355–360 vol.1.

[25] J. Jacobs, A. Averberg, and R. De Doncker, "Multiphase series resonant DC-to-DC converters: Stationary investigations," in *Proc. IEEE Power Electron. Specialists Conf. (PESC)*, Dresden, Germany, Jun. 2005, pp. 660–666.

[26] "TG-A1780," T-Global, Datasheet, www.tglobaltechnology.com.

[27] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase DC/AC converter systems," in *Proc. Energy Convers. Congr. Expo. (ECCE Asia)*, Hefei, China, May 2016, pp. 2732–2741.

[28] Z. Liao, N. C. Brooks, and R. C. Pilawa-Podgurski, "Design constraints for series-stacked energy decoupling buffers in single-phase converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7305–7308, Sep. 2018.

[29] D. Menzi, S. Weihe, J. A. Anderson, M. Kasper, J. Huber, and J. W. Kolar, "Novel S-Link enabling ultra-compact and ultra-efficient three-phase and single-phase operable on-board EV chargers," in *Proc. Control Modeling Power Electron. Workshop (COMPEL)*, ISSN: 2151-1004, Jun. 2023, pp. 1–7.