



# «X-Technologies/X-Concepts»

# *Key Enablers of Further Performance Improvements in Power Electronics*



Johann W. Kolar et al. Swiss Federal Institute of Technology (ETH) Zurich Power Electronic Systems Laboratory www.pes.ee.ethz.ch

Sept. 17, 2024







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# *Key Enablers of Further Performance Improvements in Power Electronics*



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## $\backslash$ $\overline{}$ 40 min



**Outline** 

► Introduction

**Conclusions** 

X-Technologies
 X-Concepts





#### Introduction

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Clean Energy Transition All-Electric Society







### **Decarbonization / Defossilization**

- "Net-Zero" Emissions by 2050 & Gap to be Closed
- 50 GtCO<sub>2eq</sub> Global Greenhouse Gas Emissions / Year → 280GtCO<sub>2</sub> Budget Left for 1.5°C Limit





- Human History Transition from Lower to Higher Energy Density Fuels Wood  $\rightarrow$  Coal  $\rightarrow$  Oil & Gas
- Challenge of Stepping Back from Oil & Gas to Low Energy Density Renewables







#### **Global Sea Levels by 2100**

Rising Sea Levels Due to Global Warming



• North Sea Enclosure Dyke — Mammoth Dams Envisioned to Protect 25 Million Europeans — €250bn ... €500bn







## **The Opportunity**

(2009) 16 TW-yr — 16 TW-yr (2050)



#### ■ Global Distribution of Solar & Wind Resources









Europe

#### The Approach

• CAGR of  $\approx$ 9% up to 2050  $\rightarrow$  8500 GW

Outlook of Global Cumulative Installations Until 2050 / Add. 1000 GW Off-Shore Wind Power
 In 2050 Deployment of 370 GW/Year (PV) & 200 GW/Year (On-Shore Wind) incl. Replacements



• CAGR of  $\approx$ 7% up to 2050  $\rightarrow$  5000 GW





Europe

#### **Fundamental Role of Power Electronics**

■ Global MEGA-Trends → Industry Automation | Renewable Energy | Sustainable Mobility | Urbanization etc.



- Clean Energy Transition  $\rightarrow$  "All-Electric" Society
- UN Sustainable Development Agenda  $\rightarrow$  There can be No "Plan B", because there is No "Planet B" (Ban Ki-moon)





### **Performance Indicators / Trends**





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Europe

#### **S-Curve of Power Electronics**

- « X-Technologies » / "Moon-Shot" Technologies
   « X-Concepts » → Full Utilization of Basic Scaling Laws & « X-Technologies »
- Power Electronics  $1.0 \rightarrow$  Power Electronics 4.0
- 2...5...10x Improvement NOT Only 10% !









#### X-Technologies

SiC | GaN —— 3D-Packaging & Integration Digital Signal Processing

















#### Low R<sup>\*</sup><sub>DS(on)</sub>High-Voltage Devices



• High Voltage Unipolar (!) Devices  $\rightarrow$  Excellent Sw. Performance / High Power Density





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#### Si vs. SiC Switching Behavior

- Si-IGBT  $\rightarrow$  Const. On-State Voltage Drop / Rel. Low Switching Speed, SiC-MOSFETs  $\rightarrow$  Resistive On-State Behavior / Factor 10 Higher Sw. Speed



Extremely High di/dt & dv/dt  $\rightarrow$  Challenges in Packaging / EMI







#### Monolithic 600V GaN Bidirectional/Bipolar Switch

- POWER AMERICA Program Based on Infineon's CoolGaN™ HEMT Technology (Infineon Dual-Gate Device / Controllability of Both Current Directions Bipolar Voltage Blocking Capability | Normally-On or -Off



• Analysis of 4-Quardant Operation of  $R_{DS(on)} = 140 \, m\Omega \mid 600 \, \text{V}$  Sample @  $\pm 400 \, \text{V}$ 

















#### **Circuit Parasitics**

- High di/dt
- Commutation Loop Inductance  $L_s$ Allowed  $L_s$  Directly Related to Switching Time  $t_s \rightarrow$





• Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents (Z-Matching)









#### Si vs. SiC EMI Emissions

- Higher dv/dt → Facto
   Higher Switching Frequencies → Facto
   EMI Envelope Shifted to Higher Frequencies  $\rightarrow$  Factor 10
- $\rightarrow$  Factor 10



• Higher Influence of Filter Component Parasitics & Couplings  $\rightarrow$  Advanced Design

















#### **3D-Packaging / Heterogeneous Integration**

- System in Package (SiP) Approach Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management Very High Power Density (No Bond Wires / Solder / Thermal Paste)
- PCBs Embedded Optic Fibers
- Automated Manufacturing
- Recycling (?)

2.1 in<sup>2</sup> and 34 W/in<sup>2</sup> 72 Watts





0.57 in<sup>2</sup> and 105 W/in<sup>2</sup>

60 Watts



- Future Application Up to 100kW (!)
- New Design Tools & Measurement Systems (!)
- University / Industry Technology Partnership (!)



1.26 in<sup>2</sup> and 26 W/in<sup>2</sup>











#### **Monolithic 3D-Integration**

Source: Panasonic ISSCC 2014

- GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology
- 9 Dual-Gate GaN AC-Switches
- DBM Gate Drive Transmitter Chip & Isolating Couplers
- Ultra Compact  $\rightarrow 25 \times 18 \text{ mm}^2$  (600V, 10A 5kW Motor)











- Slowing Transistor Techn. Node Scaling  $\rightarrow$  Vertical & Heterogeneous Integr. of ICs for Performance Gains
- **Extreme 3D-Integrated Cube-Sized Compute Nodes**
- Dual Side & Interlayer Microchannel Cooling



• Interposer Supporting Optical Signaling / Volumetric Heat Removal / Power Conversion

















#### **Digital Signal / Data Processing**

- Exponentially Improving uC / Storage Technology (!)
- Extreme Levels of Density (nm-Nodes) / Processing Speed
- Continuous Relative Cost Reduction



- AI-Based Design & Fully Digital Control of Complex Systems
- Distributed Intelligence / Digital Twins / Industrial IoT (IIoT)







#### **Abstraction of Power Converter Design**



- Mapping of **"Design Space"** into Converter **"η-ρ-σ-Performance Space"** Design Space Set of Selected Design- & Operating Parameters, Materials, Components, Topology, etc.







#### Multi-Objective Optimization





• *"Digital Twin"* 

• Multi-Objective Optimization  $\rightarrow$  Best Utilization of All Degrees of Freedom (!)











#### **Multi-Objective Optimization**

- Based on Mathematical Model of the Technology Mapping
   Multi-Objective Optimization → Best Utilization of the "Design Space"
   Identifies Absolute Performance Limits → Pareto Front / Surface



- Clarifies Sensitivity  $\Delta \vec{p} / \Delta k$  to Improvements of Technologies
- Trade-Off Analysis



n









#### **Design Space Diversity**

- Equal Performance \$\vec{p}\_i\$ for Largely Different Sets \$(\vec{x}, \vec{k})\_i\$ of Design Parameters
   E.g. Mutual Compensation of Volume or Loss Contributions (e.g. Cond. & Sw. Losses)



• Allows Consideration of Additional Performance Targets (e.g. Costs)







#### **Design Automation Roadmap**

- **End-to-End Horizon** Cradle-to-Grave/Cradle Modeling & Simulation
- Design for Cost / Volume / Efficiency / Manufacturing / Testing / Reliability / Recycling



• AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)









#### X-Concepts

Modularization Synergetic Association Functional Integration Hybridization Decentralization







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#### SiC/GaN Figure-of-Merit

- Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties FOM Determines Max. Achievable Efficiency @ Given Sw. Frequ.



Advantage of Multi-Level over 2-Level Converter Topologies 







#### Scaling of Multi-Cell/Level Concepts

- Reduced Ripple @ Same (!) Switching Losses Lower Overall On-Resistance @ Given Blocking Voltage Application of LV Technology to HV

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Source: R. Pilawa



 $400\,\mathrm{V}$  $\overline{u}$  $u_C$  $\frac{U}{8f_sL}$ 0 -400 V  $\Delta \hat{I}_{\max,N} = 20\,\mathrm{A}$  $\frac{1}{N^2}\Delta \hat{I}_{-}$  $\iota_L$  $\max, N=1$ 0 -20 A 10150 5 $t \, \mathrm{[ms]}$  $400\,\mathrm{V}$  $\frac{\Delta \hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32} (\frac{f_o}{f_s})^2 \frac{1}{N^3}$  $200\,\mathrm{V}$ 0 8 10 12 14 16 *f*[kHz]  $\mathbf{2}$ 6 0  $f_{sw}$  $N.f_{sw}$ 

• Scalability / Manufacturability / Standardization / Redundancy







7 Level

10

 $t \, (ms)$ 

15

**99.35%** 

2.6 kW/kg

56 W/in<sup>3</sup>

20

#### **3-Φ Hybrid Multi-Level Inverter**

- Realization of a 99%++ Efficient 10kW 3-Ф 400V<sub>rms,ll</sub> Inverter System
   7-Level Hybrid Active NPC Topology / LV Si-Technology



• 200 V Si  $\rightarrow$  200 V GaN Technology Results in 99.5% Efficiency





#### **4.8MHz GaN Half-Bridge Phase Module**

- **Combination of Series & Parallel Interleaving**
- 600V GaN Power Semiconductors,  $f_{sw}$  = 800kHz Volume of ≈180cm<sup>3</sup> (incl. Control etc.) H<sub>2</sub>0 Cooling Through Baseplate





• Operation @  $f_{out}$ =100 kHz /  $f_{sw,eff}$  = 4.8 MHz, 10 kW,  $U_{dc}$ =800V

















#### **3-Φ EV-Charger Topology**

- Isolated Controlled Output Voltage
   Buck-Boost Functionality & Sinusoidal Input Current
   Applicability of 600V GaN Semiconductor Technology
   High Power Density / Low Costs



 $\rightarrow$  Conventional / Independent OR "Synergetic Control" of Input & Output Stage







#### Synergetic Association 1/2

- 1/3-Modulation  $\rightarrow$  Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM
- Conduction Losses of the Switches ≈ -80%



• Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses







Sector I

#### Synergetic Association 2/2

- 1/3-Modulation  $\rightarrow$  Significant Red. of Losses of the Power Switches Comp. to 3/3-PWM
- Conduction Losses of the Switches ≈ -80%
- Switching Losses ≈ -70%



600

Sector I

• Operating Point Dependent Selection of 1/3-PWM OR 3/3-PWM for Min. Overall Losses

















#### **Isolated 3-ΦAC/DC Converters**

- **Conventional Approach**  $\rightarrow$  Two-Stage | 3- $\oplus$  PFC Rectifier & DC/DC Converter Stage
  - **Functional Integration**  $\rightarrow$  Utilizes AC/DC-Stage for Power Factor Corr. & HF AC Voltage Generation
    - $\rightarrow$  Transformer Stray Inductance Used as Current Source







320...530V<sub>rms</sub> Line-to-Line

**380 V**<sub>DC</sub> (260...400 V<sub>DC</sub>) Datacenter Power Distribution

- Elimination of DC/DC Converter Input Stage & DC-Link  $\rightarrow$  Single-Stage Energy Conversion (!)
- Electric Vehicle Battery Charging | Datacenter Power Supply | AC Grid Interfaces of DC Micro-Grids







#### **3-••Input DAB-Type AC/DC Converter 1/2**

Modification of 3-Φ Xfrm DAB → Prim.-Side Phase-Modular AC/DC Converter Topology
 Synchronized (!) Prim.-Side Switching @ 50% Duty Cycle



Voltage Stress on Prim.-Side AC Switches Determined by Peak Value of Grid PHASE Voltage (!) 

**Bidirectional Power Flow** 





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#### **3-••Input DAB-Type AC/DC Converter 2/2**

- Voltage Stress on AC-Side Power Transistors Determined by PHASE Voltage Amplitude (!)
- 600 V GaN MBDS for 400 VRMS Line-to-Line Grid ( $U_{L-L,pk} = 560$  V) Unity Power Factor / Bidirectional



- Power Density w/ EMI-Filter  $\approx$  6 kW/dm<sup>3</sup> (98W/in<sup>3</sup>)





#### **3-Port Resonant GaN DC/DC Converter**

- Single Transformer & Decoupled Power Flow Control
- Charge Mode PFC  $\rightarrow$  HV (250...500V) SRC DCX / Const.  $f_{sw}$ , Min. Series Inductance / ZVS Drive Mode HV  $\rightarrow$  LV (10.5...15V) 2 Interleaved Buck-Converters / Var.  $f_{sw}$  / ZVS

P = 3.6 kW



- Peak Efficiency of 96.5% in Charge Mode / 95.5% in Drive Mode
- **PCB-Based Windings** / No Litz Wire Windings  $\rightarrow$  Fully Automated Manufacturing

















#### Hybrid Integrated Active Filter (IAF) PFC Rectifier

- Hybrid Combination of Mains- and Forced-Commutated Converter 3<sup>rd</sup> Harmonic Current Injection into Phase with Lowest Voltage Phase Selector AC Switches Operated @ Mains Frequency 3-Φ Unfolder







#### Hybrid Integrated Active Filter (IAF) PFC Rectifier

- Hybrid Combination of Mains- and Forced-Commutated Converter 3<sup>rd</sup> Harmonic Current Injection into Phase with Lowest Voltage Phase Selector AC Switches Operated @ Mains Frequency 3-Φ Unfolder





• Non-Sinusoidal Mains Current

 $\rightarrow$  P<sub>0</sub>= const. Required  $\rightarrow$  Sinusoidal Mains Current  $\rightarrow$  NO (!) DC Voltage Control







 $u_{\rm c}$ 

240

6.0

7.0

8.0

9.0

300

360

#### **IAF PFC Rectifier & Buck Converter Demonstrator**



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ViPDA Europe















#### **Networking Scaling**

- Metcalfe's Law
- Moving from Hub-Based Concept to Community Concept Increases Potential Network Value Over-Proportional  $\rightarrow \sim n(n-1)$  or  $\sim n \log(n)$











#### **IIoT in Power Electronics**

Digital Twin → Physics-Based "Digital Mirror Image"
 Digital Thread → "Weaving" Real/Physical & Virtual World Together



- Requires Proper Interfaces for Models & Automated Design
   Model of System's Past/Current/Future State → Design Corrections / Predictive Maintenance etc.





#### **IIoT Starts with Sensors (!)**

- **Condition Monitoring of DC Link Capacitors** On-Line Measurement of the ESR in *"Frequency Window"* (Temp. Compensated) Data Transfer by Optical Fibre or Near-Field RF-Link





Possible Integration into Capacitor Housing or PCB

Additionally features Series Connect. Voltage Balancing









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### Smart Inverter Concept

#### Utilize High Computing Power and Network Effects in the Cloud



• On-Line Protection / Monitoring / Optimization on Component | Converter | Drive | Application Level

















#### "Moore's Law" of Power Electronics

- *"Moore's Law"* Defines Consecutive Technology Nodes Based on Min. Costs per Integrated Circuit (!) Prediction in 1965: Number of Transistors on a Chip will Double Every ≈2 Years w/ Minimal Increase in Cost



- Potential Power Density Improvement Factor 2...5 Until 2030
- Definition of " $\eta^*$ ,  $\rho^*$ ,  $\sigma^*$ ,  $f_{\rho}^*$  Technology Node" Must Consider Conv. Type / Operating Range etc. (!)







#### **Future Application / Research Areas**

- WBG Driven Extension to Medium Voltage There is Plenty of Room at the Top (SSTs, XF EV Charging etc.)
- Extreme Cost Pressure for Standardized Solutions (!)



- "There's Plenty of Room at the Bottom" (R. Feynman @ Caltech, 1959) Monolithic Integr. etc.
- Key Importance of Technology Partnerships of Academia & Industry









Source: www.roadtrafficsigns.com











#### **Power Electronics** $\rightarrow$ **Electronic** "Energy" Management

- Design Considering Converters as Standardized "Integrated Circuits" (PEBBs)
- **Extend Analysis to Converter Clusters / Power Supply Chains / etc.**



Systems" (Microgrid) or "Hybrid Systems" (Automation / Aircraft)
"Integral over Time" "Converter" "Time"

"Energy"

$$p(t) \rightarrow \int_{0}^{t} p(t) dt$$

- Power Conversion - Converter Analysis
  - $\rightarrow$  Energy Management / Distribution
  - $\rightarrow$  System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- $\rightarrow$  System Stability` (Autonom. Cntrl of Distributed Converters) - *Converter Stability* 
  - $\rightarrow$  Energy Storage & Demand Side Management → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- Costs / Efficiency

- Cap. Filtering

- etc.







#### **Energy Management** — *DC Micro-/Nanogrids*



- **Renewable Energy Integration**
- "Networked" Bidir. Flow/Exchange of Energy & Signals/Data | Distrib. Autonom. Cntrl & Protection Hybrid Power Solutions Combin. of Electric / Hydraulic / etc. Systems | Continuous Opt. & Diagnosis





**Power Electronic Systems** Laboratory





- Global Population by 2050 10bn 100 2.5 kW/Capita
   25'000 GW Installed Ren. Generation in 2050
- 4x Power Electr. Conversion btw Generation & Load
- **100'000 GW** of Installed Converter Power
- **20 Years of Useful Life**



5'000 GW<sub>eq</sub> = 5'000'000'000 kW<sub>eq</sub> of E-Waste / Year (!)
 10'000'000'000 \$ of Potential Value





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52'000'000 Tons of Electronic Waste Produced Worldwide in 2021 → 74'000'000 Tons in 2030
 Increasingly Complex Constructions → No Repair or Recycling





Growing Global E-Waste Streams  $\rightarrow$  Regulations Mandatory (!)  $\bullet$ 







Source:



#### **The Paradigm Shift**

Growing Global E-Waste Streams / < 20% Recycled

120'000'000 Tons of Global E-Waste in 2050



- *"Linear" Economy / Take-Make-Dispose → "Circular" Economy / Perpetual Flow of Resources Resources Returned into the Product Cycle at the End of Use*





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#### **Power Electronics 5.0**











# Thank you!



