Comparative Evaluation of Three-Phase SiC-Based Voltage/Current-Source Inverter Motor Drives

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***Abstract*—Variable speed drives (VSDs) operating from a common dc bus enable significant energy savings in variable-load centrifugal systems like pumps and compressors. Ideally, VSDs should provide smooth sinusoidal motor voltages to ensure compatibility with standard motors. Thus, voltage-source inverters (VSIs) equipped with an output filter or current-source inverters (CSIs) are candidate topologies. Using multi-objective Pareto optimization, this paper provides a comprehensive comparative evaluation of VSI and CSI topology and modulation variants, which employ 1200 V and/or 900 V SiC power transistors and drive a 400 V (line-to-line rms), 7.5 kW high-speed permanent magnet synchronous machine (PMSM) with a high nominal output frequency of up to 2 kHz from a 750 V dc bus. The results indicate comparable performance of VSI and CSI topologies in terms of efficiency (weighted according to the NEMA power index load profile) and power density, yet the CSI designs require larger total chip areas at least until 900 V monolithic bidirectional power transistors become available. Advantageously, the CSI's dc-side voltage-to-current conversion stage (dc-dc buck converter) can be realized with two interleaved phases that each operate in a triangular-current mode (TCM) and hence with soft-switching, while the dc-link current still shows a low ripple only; this approach clearly outperforms all other considered variants.**

***Index Terms*—Variable speed drives, voltage-source inverters, current-source inverters, multi-objective optimization.**

I. Introduction

When transitioning towards a sustainable future and limiting global warming, electric motor-driven applications play a pivotal role as they process 45% of the electrical energy consumed worldwide [1]. In certain industries, variable-load centrifugal systems like compressors, drills, pumps, and fans account for 34% to 44% of the total motor energy use [2]. However, despite their potential for energy savings through the quadratic speed-torque relationship (i.e., a power-speed relationship $P \propto \omega^3$), a major share still employs fixed-speed motors operating directly from the grid with the mechanical output power adapted to the load using valves and dampers. Thus, adopting variable speed drives (VSDs) contributes to energy savings and improves system reliability [3]–[5].

Typically, VSDs are realized as voltage-source inverters (VSIs), which, if wide-bandgap (WBG) transistors are used, should be equipped with a differential-mode (DM) and common-mode (CM) output filter as shown in **Fig. 1a**. This ensures smooth sinusoidal motor voltages, preventing issues like motor overvoltages due to reflections at the motor terminals and EMI emissions from long motor cables. Further, standard motors can be used as there are no harmonic losses, and an overall high system efficiency results [6], [7]. Alternatively, a current-source inverter (CSI) as shown in **Fig. 2a** could be employed, which benefits from its inherently sinusoidal output voltages [8], [9]. However, the CSI requires a voltage-to-current conversion stage (i.e., a buck converter) to interface a dc *voltage* bus [10].

Table I. Key specifications of the drive system.

Description	Symbol	Value	Unit
Input dc voltage	V_{dc}	750	V
Nominal motor power	P_{N}	7.5	kW
Motor voltage (l-l rms)	V_{M}	0…400	V
Motor current (rms)	I_{M}	0…12	A
Motor el. frequency	f_{M}	0…2	kHz
Phase-shift at rated power	φ	25	°

Given the growing research interest in the selection and analysis of VSD topologies [11]–[16], this paper presents a comprehensive comparative evaluation of VSI and CSI motor drives based on a multi-objective optimization (MOO) that considers several topology variants and different control/modulation methods, and the specifications in **Tab. I**. **Section II** discusses the considered topology variants and and modulations methods, **Section III** outlines the component modeling and the MOO procedure, **Section IV** compares the topologies in terms of efficiency and power density based on the MOO results, and **Section V** concludes the paper.

II. VSI and CSI Topologies and Modulation Methods

This section provides a detailed overview of the VSI and CSI topologies, and the respective modulation methods and output filter variants, which all provide differential-mode (DM) and common-mode (CM) attenuation to supply the motor with smooth sinusoidal voltages.

A. VSI with DM and CM Output Filter

Fig. 1a shows a VSI equipped with a DM and CM output filter, i.e., a "discrete full sine-wave filter" (d-FSF) [17].[1] If the dedicated CM filter components (L_{cm} and C_{cm}) are omitted, a "combined full sine-wave filter" (c-FSF) results.[2] **Fig. 1b** shows simulated key waveforms of the VSI equipped with a d-FSF and employing sinusoidal pulse-width modulation (SPWM)

[1] *Discrete* as "dedicated" filter components for DM and CM are employed, which can thus be designed independently.

[2] *Combined* because the same components (L_{dm} and C_{dm}) are used to provide DM *and* CM attenuation (dc-link referenced filter).

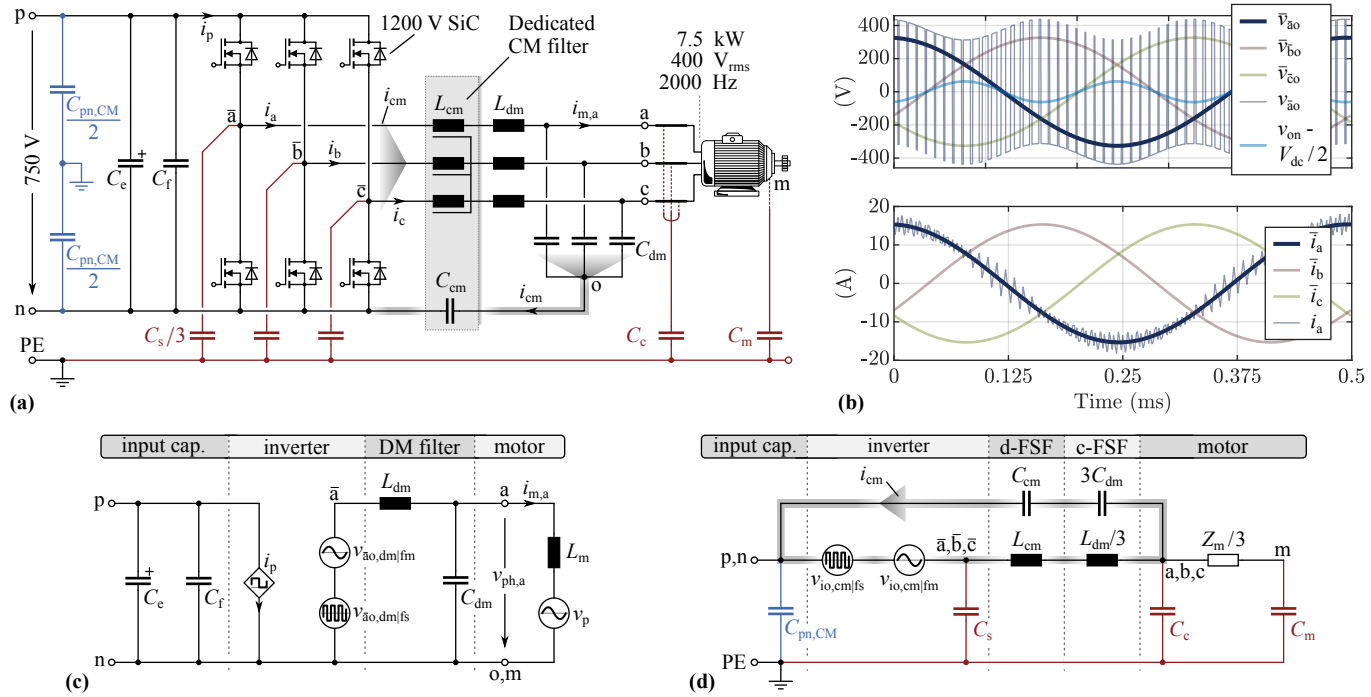

Fig. 1. **(a)** VSI with a discrete full-sine-wave filter (d-FSF) or a combined full-sine-wave filter (c-FSF), where the dedicated CM filter components L_{cm} and C_{cm} are omitted (replaced with direct connections). **(b)** Exemplary waveforms of the VSI with d-FSF using SPWM with third harmonic injection. **(c)** DM and **(d)** CM equivalent circuits (see [17] for the derivation and an in-depth discussion).

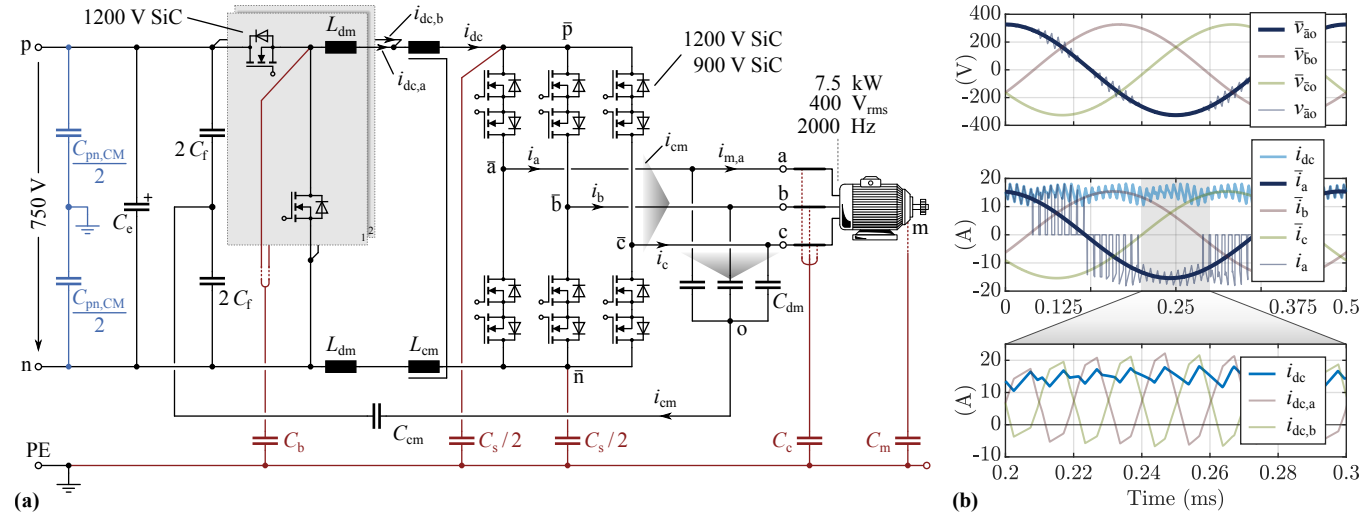

Fig. 2. **(a)** CSI with a single-phase or a two-phase (interleaved) buck converter voltage-to-current translation stage and with a DM and CM output voltage filter. **(b)** Simulated waveforms of the CSI when 2/3-PWM [18]–[20] is applied (the buck stage regulates the dc-link current to the characteristic six-pulse shape given by $\max\{|i_a|, |i_b|, |i_c|\}$, which allows clamping of one phase at all times, i.e., always only two out of three phase currents are synthesized with PWM, reducing switching losses compared to the standard 3/3-PWM modulation with constant dc-link current). The zoomed-in section highlights the soft-switching operation of the buck input stage if two interleaved phases are used: the buck inductor currents $i_{dc,a}$ and $i_{dc,b}$ change direction in each switching period to enable ZVS (i.e., the phases operate in TCM), while their sum, i.e., the dc-link current i_{dc}, advantageously remains positive and shows a relatively low ripple only.

with third harmonic injection. The inverter's switched output voltages $v_{\bar{x}o}$ are discontinuous but filtered before reaching the motor, which thus only sees the low-frequency components $\bar{v}_{\bar{x}o}$. **Fig. 1cd** show the DM and CM equivalent circuits of the VSI, which are obtained like in [17], where an in-depth explanation can be found. The DM equivalent circuit is the same for both filter configurations (c-FSF and d-FSF), whereas the CM equivalent circuit differs between the two, incorporating the dedicated CM filter components C_{cm} and L_{cm} if a d-FSF is implemented. Note that only then (with a d-FSF) modulation methods that result in a low-frequency CM voltage $v_{io,cm|fm}$, such as SPWM with third harmonic injection and discontinuous PWM (DPWM) [21], can be used; in case of a c-FSF, significant low-frequency CM currents could circulate back to the dc-link and degrade the overall system efficiency. Therefore, when optimizing the VSI with a c-FSF, only SPWM without third harmonic injection is considered. Note that the 750 V dc bus voltage mandates the use of 1200 V SiC transistors.

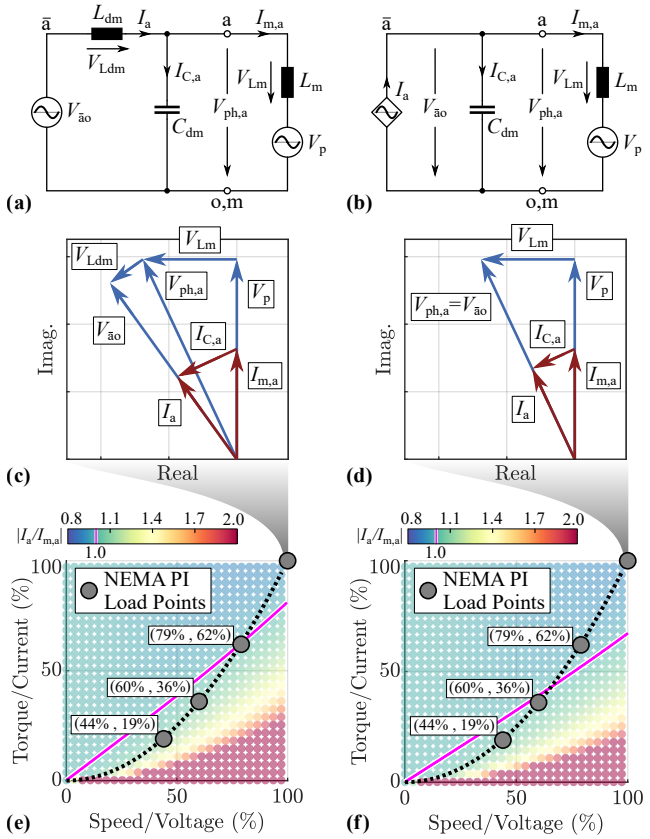

Fig. 3. Design of the DM capacitor C_{dm} to achieve reactive power compensation in the nominal operating point. Equivalent DM circuit of **(a)** the VSI and **(b)** the CSI. Resulting (first-harmonic) phasor diagrams at the nominal operating point of the motor (see **Tab. I**) for **(c)** the VSI and **(d)** the CSI. **(e)** and **(f)** show the corresponding ratios of inverter current to motor current over the operating range, and indicate the four characteristic torque-speed (current-voltage) load points used by the NEMA Power Index (PI) [22] to represent loads with a quadratic torque-speed characteristic like pumps or compressors.

B. CSI with DM and CM Output Filter

Fig. 2a shows a CSI with a DM and CM output filter [14], [23], equipped with a voltage-to-current conversion stage (i.e., a buck converter) at the input, which is needed to interface a dc voltage bus and to regulate the dc-link current i_{dc}. Whereas this buck converter stage also requires 1200 V devices, the CSI stage itself can be realized with 900 V transistors as the nominal line-to-line output voltage amplitude is only 565 V.

Advantageously, the buck converter can shape the dc-link current i_{dc} according to the characteristic six-pulse envelope of the output current absolute values as shown in **Fig. 2b** [18]–[20]. This so-called 2/3-PWM operation allows to clamp one phase at all times, i.e., the CSI transistors only operate with PWM during 2/3 of the time and with relatively low switching voltages. Compared to operation with a constant i_{dc} and hence 3/3-PWM, this reduces both, switching and conduction losses. **Fig. 2b** displays exemplary waveforms of the CSI operating with 2/3-PWM; note that the inverter's switched output *currents* i_{x} are discontinuous but filtered before reaching the motor, which thus only sees the low-frequency components $\bar{i}_{\mathrm{x}}$. Differently from the VSI in **Fig. 1a**, the voltages $v_{\bar{\mathrm{x}}\mathrm{o}}$ at the output of the CSI are inherently continuous and don't require further filtering.

Finally, the buck stage can be implemented using *two* phases that are advantageously operated in an interleaved manner. This facilitates to maintain a dc-link current i_{dc} of fixed direction and low ripple (enabling the use of convenient CSI multi-step commutation schemes based on the direction of the current [24], [25]), while the individual buck inductor currents, i.e., $i_{\mathrm{dc,a}}$ and $i_{\mathrm{dc,b}}$, show very high ripple and reverse their directions in each switching period, enabling zero-voltage switching (ZVS) to reduce switching losses, i.e., each phase operates in a triangular-current mode (TCM).

C. Reactive Power Compensation

To enhance the efficiency of both, the VSI and the CSI, the output filter capacitor C_{dm} can be designed to provide the nominal operating point reactive power required by the motor (and, in case of the VSI, of the filter inductor) as detailed in [26], [27]. Starting from the equivalent DM circuits of the VSI in **Fig. 3a** and of the CSI in **Fig. 3b**, the capacitor C_{dm} is chosen such that the fundamental component of the inverter current I_{a} is in phase with the inverter voltage $V_{\bar{\mathrm{a}}\mathrm{o}}$ in the nominal operating point, where a phase-shift of 25° between the motor current and voltage is assumed [28]–[30]. The phasor diagrams at the nominal operating point are shown in **Fig. 3cd** for the VSI and the CSI, respectively. Clearly, despite the high operating frequency and the thus comparably high reactive power demand of the motor, the inverter delivers only active power, resulting in a lower inverter current compared to the motor current. Since the compensation is designed for the nominal operating point but a VSD operates across varying speeds and torques (voltages and currents), **Fig. 3ef** indicate the ratio of the inverter current amplitude I_{a} to the motor current amplitude $I_{\mathrm{m,a}}$ over the operating range. Note that **Fig. 3ef** also reports the typical torque-speed characteristic of a pump or compressor application, including the representative load points for such loads (i.e., as used to define the NEMA Power Index (PI) [22]). Clearly, in this example, the reactive power compensation leads to a lower inverter current for operating points that are close to the design point (i.e., the nominal operating point), which is relevant for the selection of the power transistors.

III. Multi-Objective Optimization Framework

To comprehensively assess the performance limits of VSI and CSI motor drives in terms of efficiency and power density, we employ a MOO routine like in [31] (there, also further details on the process and the component models are given, which are not reiterated here for the sake of brevity) to model and evaluate the possible realization variants of the VSI and the CSI described in **Section II**. The implemented MOO framework is explained using the flowchart in **Fig. 4**, considering the VSI with a c-FSF as an example. The optimization process is applied to each relevant combination of topology and modulation, considering the specifications in **Tab. I** and a typical high-speed permanent magnet synchronous machine (PMSM) with a $\varphi = 25°$ phase-shift between voltage and current at rated power [28]–[30].

A. System Model

On the system level, each topology has two main degrees of freedom (DOF): the switching frequency f_{sw} and the inductor current ripple Δi_L. For a given combination of f_{sw} and Δi_L, the optimization routine designs the DM inductor L_{dm} to achieve the specified ripple Δi_L; the DM capacitor C_{dm} to compensate for the motor and filter reactive power as discussed in **Section II-C**; and the CM capacitor C_{cm} to limit the peak of the low-frequency CM current to 10 mA. Afterwards, to ensure that the output voltage ripple Δv_C (zero-to-peak) remains below 3.5 % of the line-to-neutral output voltage amplitude, the spectra of the inverter's high-frequency output quantities ($v_{\bar{a}o,dm|fs}$ and $v_{io,cm|fs}$ for the VSI in **Fig. 1cd**) are analyzed. Assuming in-phase DM and CM noise, 1.75 % of the ripple budget is allocated to DM noise and 1.75 % to CM noise. The CM choke L_{cm} is then designed to set the resonance frequency between L_{cm} and C_{cm}, limiting the amplitudes of the high-frequency CM voltage harmonics at the motor side to 1.75 %. Finally, the previously-calculated DM capacitor C_{dm}, is checked to be sufficiently large to keep the harmonics' amplitudes of the high-frequency DM voltage at the motor side below 1.75 %. If this condition is not met, the DM capacitor is increased to satisfy the output voltage ripple requirement.[3] Note that C_{cm} and L_{cm} are included in the optimization routine only for the topologies with a dedicated CM filter (d-FSF). Ultimately, designs with DM and/or CM resonance frequencies too close to the output frequency (within a factor of 4) are discarded. With all circuit elements defined, the algorithm calculates the idealized electrical waveforms over one fundamental period at the nominal operating point, where (for the considered load profile) the highest component stresses occur.[4] Based on these waveforms the components are designed.

B. Component Models

Transistors: Considering 1200 V and 900 V baseline devices (Wolfspeed C3M0016120K and C3M0010090K, respectively), the conduction losses are modeled using the temperature-dependent on-resistance R_{on}, while the switching losses are based on calorimetrically measured data from [32] and [33], respectively. The chip-area is a device-level DOF adjusting the trade-off between conduction and switching losses: the number of parallel-connected transistors, N_{par}, is varied (including $N_{par} < 1$, which corresponds to transistors with higher R_{on} than the considered baseline devices). Additionally, different design junction temperatures are considered, as lower temperatures facilitate lower losses but require larger heatsinks.

Heatsink: The thermal interface between transistors and heatsink is modeled with a typical thermal impedance of 0.3 K in^2/W, and the heatsink volume is obtained assuming a cooling-system performance index [34] of $CSPI = 10\,\mathrm{W/(dm^3K)}$ and an ambient temperature of $T_a = 40°C$.

[3]This results in over-compensation of the motor's reactive power at rated power, requiring additional reactive power from the inverter as well.

[4]In contrast, for servo drives, operating points at full torque but (almost) zero speed/voltage could be critical regarding the thermal design.

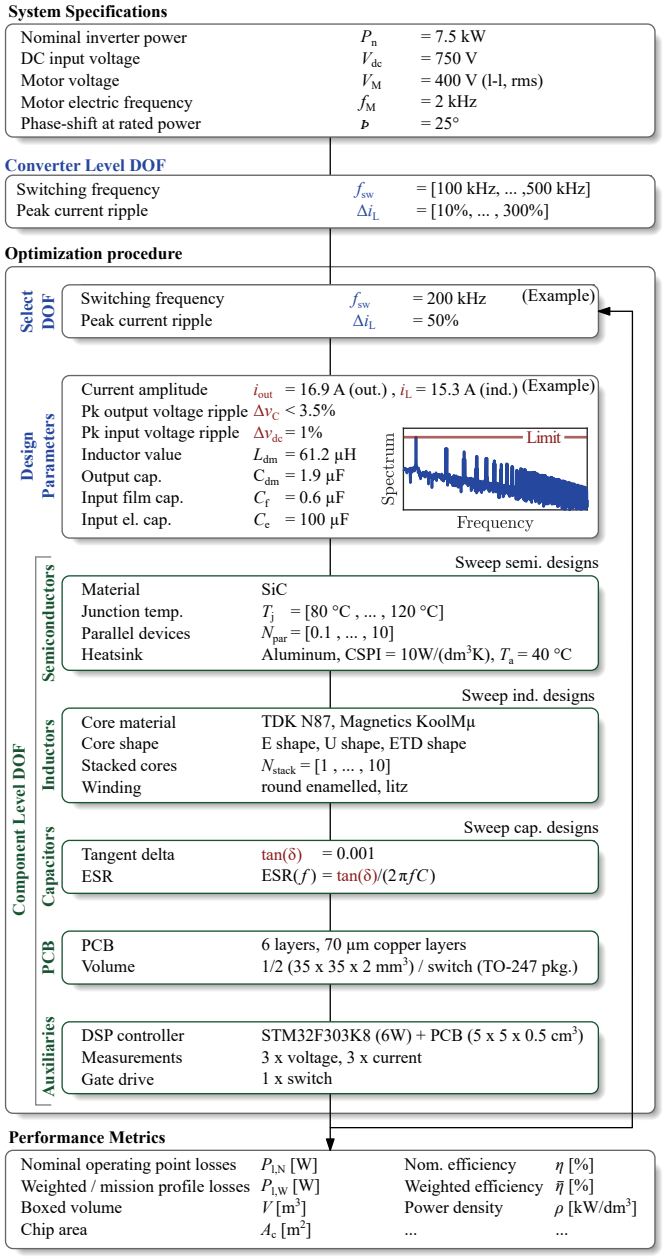

Fig. 4. Flowchart of the multi-objective optimization (MOO) routine implemented in MATLAB for the example of a VSI with c-FSF; like flowcharts could be drawn for the other topology variants.

Filter inductors: The design tool from [35] is employed to optimize the inductors by varying the component-level DOF like core material (N87, Magnetics KoolMµ), core size, winding (solid/litz wire), etc.

CM choke: Optimized based on the model presented in [36], considering nanocrystalline core material (Vitroperm 500) and exploring various component-level degrees of freedom, such as core size and winding type (solid or litz wire).

Capacitors: The volumes of the ac-side DM capacitor C_{dm} and the dc-side film capacitor C_f (designed for a maximum high-frequency zero-to-peak ripple of 1 %) are found considering typical volumetric energy densities of commercially available film capacitors. Even though the film capacitor losses are very

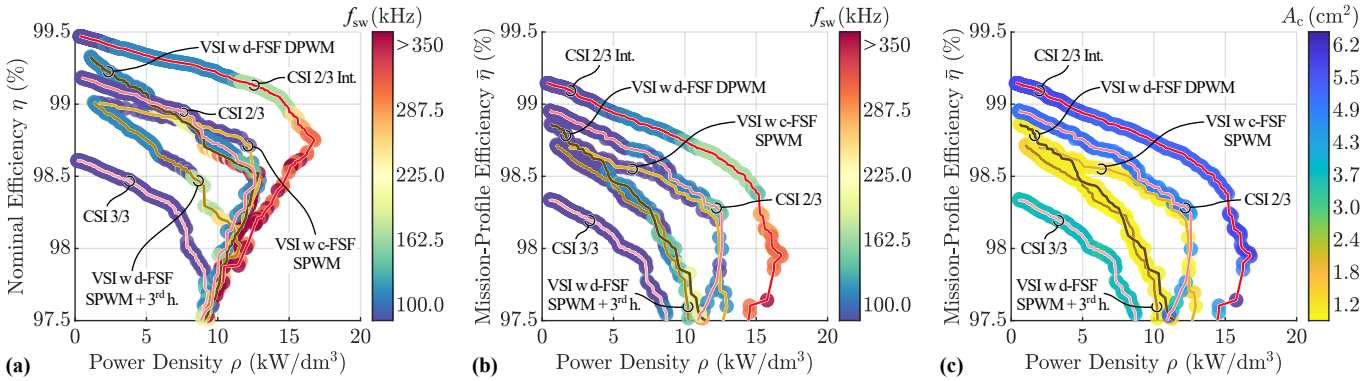

Fig. 5. Comparative evaluation of the analyzed topologies and modulation methods: **(a)** Nominal efficiency vs. power density with color-coded switching frequency; **(b)** weighted efficiency (equal weight for the NEMA PI load points in **Fig. 3ef**) vs. power density with color-coded switching frequency; **(c)** weighted efficiency vs. power density with color-coded total chip area.

small, they are considered via $\tan\delta = 0.001$. On the dc-side, an additional bulk electrolytic capacitor C_e is considered similarly. Dedicated CM capacitors, if any, are neglected due to their small size and losses.

PCBs and auxiliaries: The power PCB area/volume depends on the number of parallel transistors and the package size. For the control PCB, a fixed area is assumed based on experience; similarly, the auxiliary losses are estimated at 6 W and are assumed constant across all topologies.

C. Performance Evaluation

For a given combination of system-level DOF, i.e., (f_{sw}, Δi_L), the optimization routine recombines all feasible component realizations to obtain all feasible converter realizations. The component stresses at the three remaining NEMA PI load points (shown in **Fig. 3ef**) are evaluated and converter realizations that overstress a component are discarded. Finally, performance metrics like nominal efficiency η, boxed volume V (considering 50 % air between components), power density ρ, mission-profile efficiency $\bar{\eta}$ (based on the NEMA PI load points shown in **Fig. 3ef**), total chip area A_c, etc. are calculated.

IV. Multi-Objective Optimization Results

Fig. 5 presents a comparative analysis of the performance limits of the considered VSI and CSI topologies and modulation methods. For each variant, **Fig. 5a** shows the corresponding efficiency vs. power density η-ρ Pareto front, and **Fig. 5b** considers a weighted mission profile efficiency $\bar{\eta}$ instead (NEMA PI load profile for variable loads with quadratic torque-speed characteristics like pumps or compressors, i.e., operating points shown in **Fig. 3ef** weighted equally). The color scale represents the switching frequency f_{sw}. Interestingly, a VSI using a c-FSF, a VSI using a d-FSF with DPWM, and a CSI using 2/3-PWM with a single-phase buck voltage-to-current conversion stage exhibit similar performance, with largely overlapping Pareto fronts in the η-ρ plane.

However, when the mission-profile efficiency is considered (Pareto fronts in the $\bar{\eta}$-ρ plane in **Fig. 5b**), the VSI with a d-FSF and DPWM is not competitive anymore, whereas the CSI using 2/3-PWM and a single-phase buck dc-dc stage shows slightly higher efficiency than the c-FSF VSI with the same power density. In both cases, a CSI with 3/3-PWM shows clearly lower efficiency and power density due to higher switching and conduction losses, which result in larger heatsinks [20].

Finally, a 2/3-PWM CSI using an interleaved soft-switched two-phase buck dc-dc converter ("CSI 2/3 Int." in **Fig. 5**) clearly outperforms all other variants. This superior performance is attributed to lower switching losses in the buck converter, as it achieves soft-switching through TCM operation of the individual phases while, advantageously, the dc-link current of the CSI still only shows a relatively low ripple (see **Fig. 2**).

Fig. 5c shows again the $\bar{\eta}$-ρ Pareto fronts of the analyzed topologies, but the color scale indicates the total chip area used in each design. Notably, the best performing (i.e., Pareto-optimal) VSI variants use less chip area compared to the Pareto-optimal CSI variants, which reflects the higher switch count of the CSI topologies (anti-series connection of transistors in the CSI stage, additional buck dc-dc converter stage). It is important to highlight that the performance of the VSI variants can not be improved by investing more chip area due to the associated increase in switching losses. Note further that future monolithic bidirectional transistors in the 900 V or 1200 V class [37] would heavily reduce the CSI chip area usage.

V. Conclusion

Variable speed drives (VSDs) facilitate significant energy savings in applications like pumps or compressors. Here, we compare different realization options of 7.5 kW VSDs operating from a 750 V dc bus and driving a high-speed PMSM with an electrical frequency of up to 2 kHz. Ideally, VSDs provide sinusoidal motor voltages, i.e., voltage-source inverters (VSIs) must be equipped with an output filter. Alternatively, current-source inverters (CSIs) can be used but require a dc-side buck converter stage for the voltage-to-current conversion. The implemented multi-objective optimization routine identifies similar performance regarding power density and (mission-profile) efficiency of certain VSI and CSI variants (specifically when the CSI utilizes its dc-side buck converter to enable 2/3-PWM operation). Finally, implementing the buck converter stage with two interleaved phases operating in triangular-current mode (TCM) to achieve soft-switching results in a low dc-link

current ripple and clearly provides the best efficiency and/or power density among all considered variants.

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