Novel Single-Stage High-Frequency-Isolated Four-Switch Bidirectional Single-Phase PFC Rectifier

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***Abstract*—Power Factor Correction (PFC) rectifiers supplying a dc bus common for several variable speed motor drives should provide galvanic isolation and bidirectional power flow capability. State-of-the-art topologies often suffer from two-stage power conversion and/or high active component count. Therefore, this paper investigates a novel single-phase single-stage high-frequency-isolated PFC rectifier with non-pulsating input current and low active component count, i.e., only four standard power transistors with well-defined blocking voltages. The paper systematically explains the operating principle, and derives the main power component voltage and current stresses resulting in design guidelines for the realization of a 2.5 kW prototype system interfacing the European 230 V (rms) single-phase ac grid and an isolated 400 V dc output, which achieves an estimated nominal efficiency close to 96%. Further, the paper details the closed-loop control strategy and proposes a start-up procedure, which are both verified by means of circuit simulations.**

I. Introduction

Power Factor Correction (PFC) rectifiers supplying a standard 400 V dc bus for one or several variable speed motor drives from a 50 Hz, 230 V (rms, line-to-neutral) European single-phase ac grid are required to feature (a) galvanic isolation to enable a flexible grounding of the motor drive inverters and (b) bidirectional power flow to facilitate regenerative braking of the motors [1], [2]. A standard approach to generate such an isolated dc bus voltage employs a two-stage system, i.e., a non-isolated ac-dc front-end PFC rectifier stage and a subsequent High-Frequency (HF) isolated dc-dc converter stage (see **Fig. 1a**) [3]–[5]. This, however, suffers from high realization effort and component count, and the fact that the power is converted twice ultimately limits the efficiency. Alternatively, single-stage PFC rectifier topologies with HF isolation could be employed, but known topologies [6]–[12] show specific disadvantages: The concepts from [6]–[9] require power transistors with bipolar voltage blocking capability, [9] and [10] allow unidirectional power flow only, and variants like [11], [12] require an excessive number of power transistors.

Current research therefore aims at identifying new single-phase single-stage HF-isolated PFC rectifiers with low active component count and low complexity. Based on a systematic method for generating new power converter circuit topologies, [13] has proposed the novel converter circuit depicted in **Fig. 1b**: Advantageously, the required functionality, i.e., PFC, HF isolation, and single-stage power conversion, can be achieved with only four standard power transistors subject to well-defined blocking voltages. However, [13] does not give a detailed description of the operating principle and the control concept, nor design guidelines. Thus, this paper provides all relevant aspects for a practical realization of this new converter topology. First, **Section II** systematically derives the operating principle.

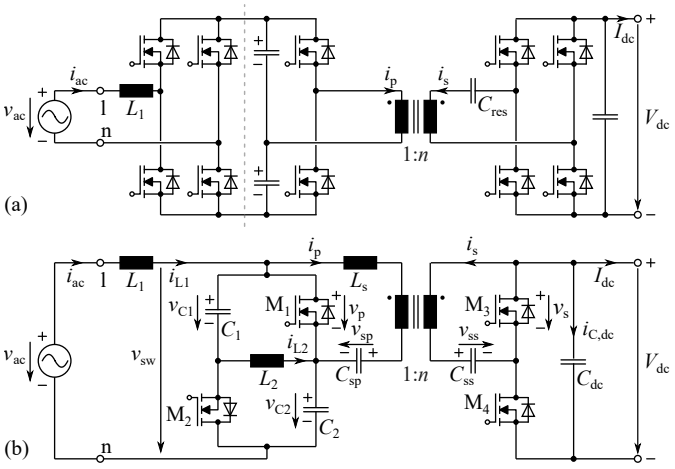

Fig. 1. Single-phase HF-isolated PFC rectifier topologies: **(a)** State-of-the-art topology with two-stage power conversion (i.e., a PFC rectifier front-end and an isolated dc-dc stage) and **(b)** novel single-stage PFC rectifier with HF isolation and low active component count proposed in [13].

Table I: System Specifications.

Parameter	Variable	Value	Unit
ac voltage (line-to-neutral)	$V_{\mathrm{ac,rms}}$	230	V
ac frequency	f_{ac}	50	Hz
dc voltage	V_{dc}	400	V
dc output power	P_{dc}	2.5	kW

Section III presents design guidelines for the specifications in **Tab. I** and discusses the main system-level trade-offs. Further, **Section IV** details the control strategy and proposes a start-up sequence. **Section V** verifies the converter operation with detailed simulation results. Finally, **Section VI** summarizes the main findings and provides an outlook on future research.

II. Operating Principle

This section discusses the operating principle of the proposed single-phase PFC rectifier depicted in **Fig. 1b**. Based on the conceptual voltage and current waveforms provided in **Fig. 2**, first, the grid current formation and subsequently the HF-isolated power transfer are discussed.

A. Grid Current Formation

On the grid input side, the converter in **Fig. 1b** comprises an ac switching cell with two standard power transistors M_1, M_2 with unipolar voltage blocking capability (realized, e.g., with SiC MOSFETs), two capacitors C_1, C_2, and an auxiliary inductor L_2.

Note that the power transistors M_1 and M_2 show opposing blocking voltage directions and thus the capacitor voltages v_{C1}, v_{C2} are limited to strictly positive and strictly negative

values, respectively. The two power transistors M_1, M_2 are switched complementarily (the two conduction states (i) and (ii) are indicated in **Fig. 3**), resulting in an instantaneous ac-side switched voltage of

$$v_{\rm sw} = \begin{cases} v_{\rm C2} < 0, & s_1 = 1 \\ v_{\rm C1} > 0, & s_1 = 0, \end{cases} \tag{1}$$

where s_1 is the gate signal of switch M_1. Both capacitor voltages consist of an ac component (impressed by the grid with an amplitude $\frac{\hat{V}_{\rm ac}}{2}$; see **Fig. 2a**) and a dc offset voltage $\frac{V_{\rm off}}{2}$ defining the blocking voltage of the power transistors M_1 and M_2 as

$$V_{\rm off} = v_{\rm C1} - v_{\rm C2}. \tag{2}$$

The aim of any PFC rectifier is to impress a sinusoidal grid current $i_{\rm ac}$ in phase with the grid voltage $v_{\rm ac}$ and with an amplitude $\hat{I}_{\rm ac} = \frac{2P_{\rm dc}}{\hat{V}_{\rm ac}}$ as highlighted in **Fig. 2d**. This is realized here by setting the local average value of the ac-side voltage $v_{\rm sw}$ (see **Fig. 2c**) to $\langle v_{\rm sw}\rangle \approx v_{\rm ac}$ (i.e., assuming negligible mains-frequency voltage drop across L_1) by adjusting the relative on-time $d \in [0,1]$ of the power transistor M_1 with

$$d \approx \frac{v_{\rm C1} - v_{\rm ac}}{v_{\rm C1} - v_{\rm C2}} = \frac{v_{\rm C1} - v_{\rm ac}}{V_{\rm off}}, \tag{3}$$

as shown in **Fig. 2b**. To maintain grid-current controllability, the ac switching cell is constrained to capacitor voltages $v_{\rm C1}(t) > v_{\rm ac}(t)$ and $v_{\rm C2}(t) < v_{\rm ac}(t)$ according to (1), i.e., is limited to boost operation[1] with $V_{\rm off} \geq \hat{V}_{\rm ac}$ and the resulting minimum duty-cycle margin within a grid period $T_{\rm ac}$ is defined as

$$\Delta d = \frac{1}{2}\left(1 - \frac{\hat{V}_{\rm ac}}{V_{\rm off}}\right). \tag{4}$$

Last, an auxiliary inductor L_2 balances the voltages of the capacitors C_1 and C_2. The current $i_{\rm L2} = -i_{\rm L1}$ establishes naturally and comprises a Low-Frequency (LF) and an HF component (**Fig. 2d**).

B. Isolated High-Frequency Power Transfer

The power circuit in **Fig. 1b** further comprises an HF transformer (turns-ratio n and ac-input-side related series inductance $L_{\rm s}$), series capacitors $C_{\rm sp}$ and $C_{\rm ss}$, and a dc-side half-bridge with the power transistors M_3, M_4. The operation of the ac switching cell performing grid current formation results in a voltage across the power transistor M_1 of

$$v_{\rm p} = \begin{cases} 0, & s_1 = 1 \\ V_{\rm off}, & s_1 = 0, \end{cases} \tag{5}$$

which is applied to the series connection of the transformer's primary-side winding and the series capacitor $C_{\rm sp}$. The series capacitor $C_{\rm sp}$ blocks the LF voltage component $\langle v_{\rm p}\rangle \approx (1-d)\cdot V_{\rm off} \approx v_{\rm sp}$ and the HF component $\tilde{v}_{\rm p} = v_{\rm p} - \langle v_{\rm p}\rangle$ is applied to the transformer as indicated in **Fig. 4a**.

Similarly, the dc-side voltage $v_{\rm s} \in \{0, V_{\rm dc}\}$ (i.e., the voltage across M_3) comprises an LF $\langle v_{\rm s}\rangle$ and an HF component $\tilde{v}_{\rm s}$. Aiming at a Dual Active Bridge (DAB)-type power transfer, the transistors M_3, M_4 replicate the primary-side switching pattern but with a Pulse-Width Modulation (PWM) carrier phase shift $g \in [-1,1]$. **Fig. 3** highlights the ac-side (i), (ii) and dc-side conduction states (a), (b), resulting in four switching states of the converter. **Fig. 4a** shows the phase-shifted transformer voltages during two switching periods $T_{\rm sw} = 1/f_{\rm sw}$.

[1]Note that this limit only applies to the relationship between the grid voltage amplitude $\hat{V}_{\rm ac}$ and the (internal) offset voltage $V_{\rm off}$. However, the dc output voltage $V_{\rm dc}$ can be freely selected to any value larger or smaller than $\hat{V}_{\rm ac}$, i.e., the system shows buck-boost capability.

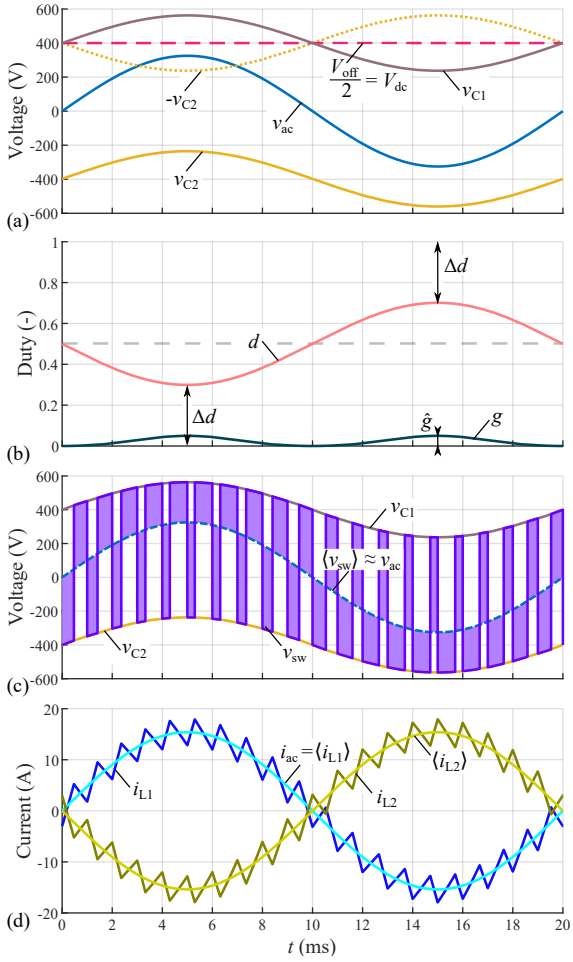

Fig. 2. Conceptual waveforms of the proposed single-phase PFC rectifier from **Fig. 1b** for one grid period $T_{\rm ac}$ with offset voltage $V_{\rm off} = 800\,\rm V$, transformer turns ratio $n = 0.5$, $V_{\rm dc} = 400\,\rm V$ and $P_{\rm dc} = 2.5\,\rm kW$: **(a)** Grid voltage $v_{\rm ac}$, capacitor voltages $v_{\rm C1}$, $v_{\rm C2}$ and offset voltage $\frac{V_{\rm off}}{2}$, **(b)** duty cycle d and DAB phase shift g (cf. (8)), **(c)** switched voltage $v_{\rm sw}$, voltages $v_{\rm ac}$, $v_{\rm C1}$, $v_{\rm C2}$, **(d)** LF grid current $i_{\rm ac}$ and inductor currents $i_{\rm L1}$, $i_{\rm L2}$.

The difference between the primary-side voltage $\tilde{v}_{\rm p}$ and the primary-side-related secondary-side transformer voltage $\tilde{v}'_{\rm s}$ is applied to the transformer series inductance $L_{\rm s}$ and results in the characteristic trapezoidal transformer current $i_{\rm p}$ as shown in **Figs. 4b,c**. To minimize the current stress of the transformer and the power transistors, here the transformer turns ratio n is advantageously selected to match the primary-side voltage $v_{\rm p} = \{0, V_{\rm off}\}$ and secondary-side voltage $v_{\rm s} = \{0, V_{\rm dc}\}$ with

$$n = \frac{V_{\rm dc}}{V_{\rm off}} = \frac{V_{\rm dc}}{v_{\rm C1} - v_{\rm C2}}. \tag{6}$$

As derived in [13], the absolute value of the HF power flow $|p_{\rm t}|$ is—similar to a dc-dc DAB converter—defined as

$$|p_{\rm t}| = \frac{V_{\rm off} V_{\rm dc}}{2 f_{\rm sw} L_{\rm s} n} \cdot \left(2d\,(1-d)\,|g| - g^2\right), \tag{7}$$

where $g > 0$ results in positive (from the grid to the dc output)

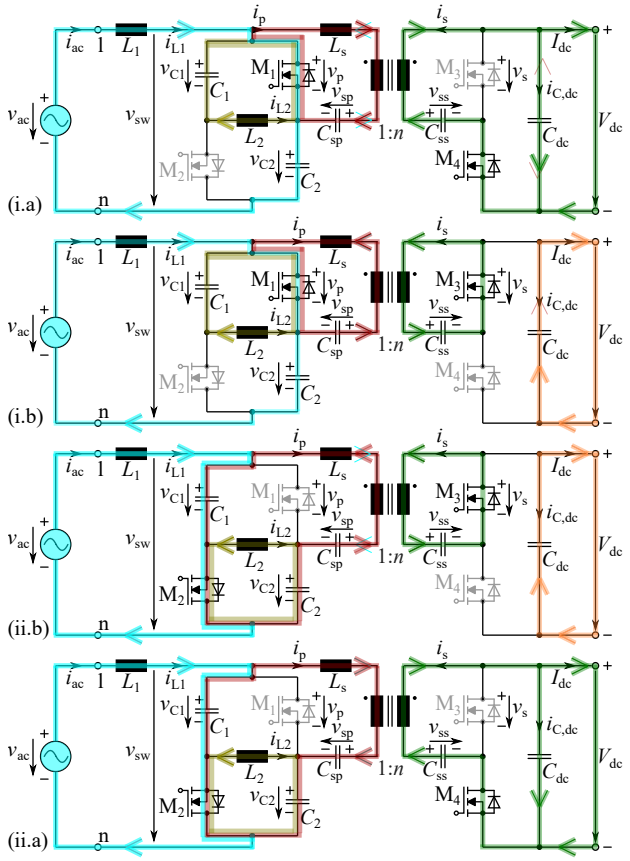

Fig. 3. Switching states and conduction paths at the beginning of each time interval in **Fig. 4**: **(i.a)** $s_1 = 1, s_4 = 1$, **(i.b)** $s_1 = 1, s_3 = 1$, **(ii.b)** $s_2 = 1, s_3 = 1$, **(ii.a)** $s_2 = 1, s_4 = 1$, where $s_1 \ldots_4 \in \{0, 1\}$ are the gate signals of the corresponding switches. The switches M_1, M_2 are switched complementarily, as are M_3, M_4; note that (i) and (ii) refer to the switching state of the ac-side and (a) and (b) to that of the dc-side.

and and $g < 0$ in negative power flow values p_t.

In order to allow small ac-side filter capacitors C_1 and C_2 (i.e., for HF filtering only), the time-varying grid input power $p_{ac} = v_{ac} i_{ac}$ shown in **Fig. 4d** needs to be transferred to the dc side, i.e., $p_t \approx p_{ac} \in [0, 2P_{dc}]$ is required. This is realized with an LF time-varying PWM carrier phase shift absolute value

$$|g| = d - d^2 - \sqrt{d^4 - 2d^3 + d^2 - \frac{2 f_{sw} L_s |p_t| n}{V_{off} V_{dc}}}, \qquad (8)$$

as indicated in **Fig. 2b**. Note that the maximum HF power transfer is obtained at $|g| = g_{max} = \Delta d(1 - \Delta d)$ (see **Fig. 2b**) and the equation is valid for $|g| < \min(d, 1 - d)$. The resulting instantaneous LF and HF transformer power flow is presented in **Fig. 4d** and locally resembles that of a dc-dc DAB converter but the local average value varies across the grid period T_{ac} as intended.

III. PFC Rectifier Design Guidelines

The goal of this section is to provide detailed design guidelines for the realization of a 2.5 kW converter hardware according to the system specifications in **Tab. I** by identifying suitable power components, i.e., the characteristic values for the capacitors C_1, C_2, C_{sp}, C_{ss}, C_{dc}, the inductors L_1, L_2, the HF transformer, and the power transistors $M_1 \ldots M_4$. **Tab. II** summarizes the selected parameters. Here, a typical switching

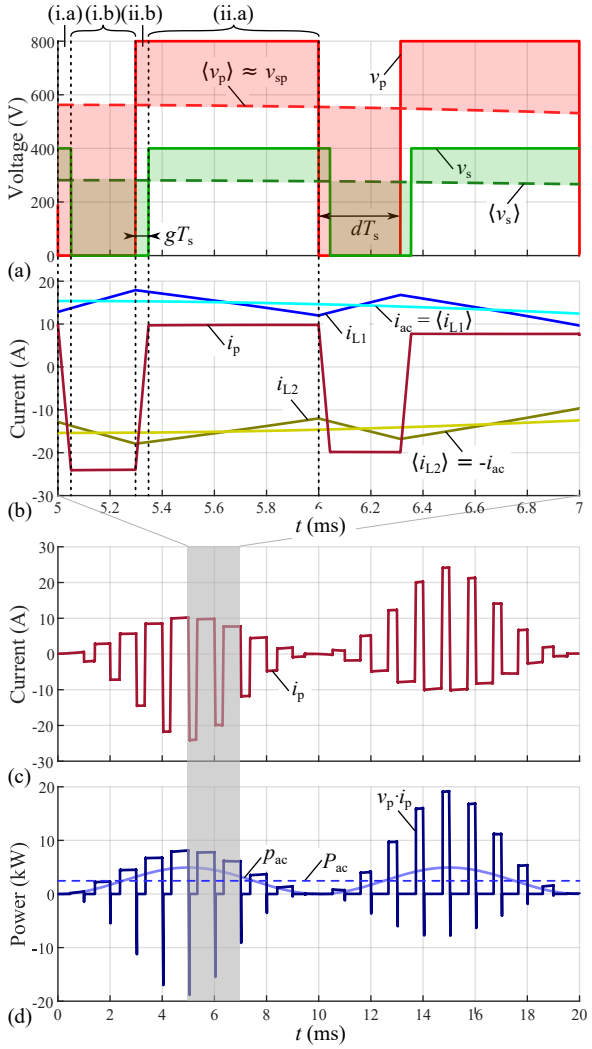

Fig. 4. Conceptual waveforms for two switching periods T_{sw} at $t = 5$ ms in **Fig. 2**: **(a)** DAB voltages (for $n = 0.5$) v_p (with a LF $\langle v_p \rangle$ and HF component $\tilde{v}_p$) and v_s (with a LF $\langle v_s \rangle$ and HF component $\tilde{v}_s$). Also indicated are the four switching states (i.a), (i.b), (ii.b) and (ii.a) as illustrated in **Fig. 3**. **(b)** LF grid current i_{ac}, inductor currents i_{L1}, i_{L2} and transformer current i_p. Conceptual HF power transfer key waveforms for one grid period T_{ac}: **(c)** Transformer current i_p, **(d)** DAB power $v_p \cdot i_p$, input power p_{ac} and average power $P_{ac} = P_{dc}$ (output power).

frequency of $f_{sw} = 72$ kHz is considered such that only the 3rd switching-frequency harmonic component at 216 kHz falls within the band starting at 150 kHz where conducted Electromagnetic Interference (EMI) limits apply.

A. AC Switching Cell Passives

The inductors L_1 and L_2 are subject to the same voltage and current stresses, thus, their inductance values are chosen to be identical. The maximum current ripple occurs for $d = 0.5$, and to limit the peak (i.e., 1/2 peak-to-peak) HF current ripple $k_{i,pk} = 20\%$ relative to the maximum LF inductor current $\hat{I}_{ac} = 15.4$ A, the required inductance values can be approximated with

$$L_1 = L_2 = \frac{1}{8} \frac{V_{off}}{k_{i,pk} \cdot \hat{I}_{ac} \cdot f_{sw}}. \qquad (9)$$

$L_1 = L_2 = 450\,\mu$H results for the offset voltage of $V_{off} = 800$ V selected in **Section III-B**.

TABLE II: MAIN PFC RECTIFIER PARAMETERS.

Parameter	Variable	Value	Unit
Switching frequency	$f_{\rm sw}$	72	kHz
Primary-side inductors	L_1, L_2	450	µH
ac-side capacitors	C_1, C_2	6	µF
Offset voltage	$V_{\rm off}$	800	V
Transformer turns ratio	n	0.5	
Transformer series/leakage inductance	$L_{\rm s}$	16.5	µH
Transformer magnetizing inductance	$L_{\rm m}$	1.65	mH
Series capacitor ac-side	$C_{\rm sp}$	3	µF
Series capacitor dc-side	$C_{\rm ss}$	12	µF
dc capacitor	$C_{\rm dc}$	2	mF

Similarly, the capacitors C_1 and C_2 are subject to the same voltage and current stresses, and identical capacitance values are required to assure an equal grid voltage sharing. The value of the capacitors $C_1 = C_2$ is chosen such that, first, an HF voltage ripple criterion is met, and, second, the impact on the HF DAB power transfer is negligible.

The first criterion is implemented by a peak HF voltage ripple limit $k_{\rm v,pk} = 5\%$ relative to the maximum LF voltage $\hat{V}_{\rm C} = \frac{1}{2}(V_{\rm off} + \hat{V}_{\rm ac})$ (see **Fig. 2a**), i.e.,

$$C_1 = C_2 = \frac{(1-\Delta d)\cdot \hat{I}_{\rm ac}}{2k_{\rm v,pk}\hat{V}_{\rm C} f_{\rm sw}}, \tag{10}$$

resulting in a minimum capacitance value of 2.7 µF.

The second criterion requires a switching-frequency impedance $Z_{\rm C1}(f_{\rm sw})$ substantially below the impedance of the series capacitor $Z_{\rm sp}(f_{\rm sw})$ and here a minimum ratio $C_1/C_{\rm sp} \geq 2$ is enforced. With a series capacitor of $C_{\rm sp} = 3\,\mu$F selected in **Section III-B**, the second criterion dominates and the required capacitance $C_1 = C_2 = 6\,\mu$F ensures a relative HF peak voltage ripple of only $k_{\rm v,pk} < 3\%$.

B. Isolated High-Frequency Power Transfer

The parameters relevant for the HF DAB power flow need to be selected such that the time-varying power flow $p_{\rm t} \in [0, 2P_{\rm dc}]$ can be assured. There, the ac switching cell offset voltage $V_{\rm off}$ (2), is a key parameter which impacts the maximally possible DAB power transfer $p_{\rm t}$ in two ways: Not only does $V_{\rm off}$ directly influence $p_{\rm t}$ (7), but $V_{\rm off}$ also defines the duty cycle margin Δd according to (4) (see **Fig. 2b**, **Fig. 5a**) and thus—via the maximum PWM carrier phase shift $|g| < \min(d, 1-d) \leq \Delta d$—indirectly limits the maximally possible DAB power transfer.

Note that the minimum duty cycle margin Δd (4) and the maximum required power flow $p_{\rm t,max} = p_{\rm ac,max} = 2P_{\rm dc}$ occur simultaneously at $t = 5\,$ms (see **Fig. 2**). When maintaining the optimal transformer turns ratio n (6), an upper bound for the series inductance value, $L_{\rm s,max}$, can be derived from (7) as

$$L_{\rm s,max} = \frac{V_{\rm off}^2}{2f_{\rm sw}p_{\rm t,max}} \cdot \Delta d^2 \cdot (1-\Delta d)^2, \tag{11}$$

with the maximum peak-power PWM phase shift $\hat{g} = \hat{g}_{\rm max} = \Delta d(1-\Delta d)$. Further, to avoid extremely low phase shift values g (with potentially negative impact on the power flow controllability due to the impact of delay and PWM interlock times), a lower bound $L_{\rm s,min}$ is also derived from (7) by defining a minimum peak-power phase shift $\hat{g}_{\rm min}$ as

$$L_{\rm s,min} = \frac{V_{\rm off}^2}{2f_{\rm sw}p_{\rm t,max}} \cdot (2\Delta d|\hat{g}_{\rm min}| - 2\Delta d^2|\hat{g}_{\rm min}| - \hat{g}_{\rm min}^2). \tag{12}$$

TABLE III: CONSIDERED POWER TRANSISTORS.

Pt. Number	Ref.	Rated Volt.	$R_{\rm nom}$
C3M0016120K	[16]	1200 V	16 mΩ
C3M0010090K	[17]	900 V	10 mΩ
IMZA65R027M1H	[18]	650 V	27 mΩ

Here, $\hat{g}_{\rm min} = 5\%$ is considered, which corresponds to a time interval of 700 ns (for $f_{\rm sw} = 72\,$kHz). However, the choice of $g_{\rm min}$ ultimately depends on the clock frequency of the controller and might need to be increased to ensure sufficient power flow resolution.

Fig. 5b depicts $L_{\rm s,min}$ and $L_{\rm s,max}$ as a function of the offset voltage $V_{\rm off}$, thus defining the design space for the series inductance $L_{\rm s}$ which is ideally realized by the transformer leakage inductance and can be tuned as explained in [14], [15]; note that a typical ratio of transformer leakage and magnetizing inductance of $L_{\rm s}/L_{\rm m} = 1\%$ is considered.

Figs. 5c,d further investigate the resulting rms and peak transformer currents $I_{\rm p,rms}$ and $\hat{I}_{\rm p}$, respectively, depending on the offset voltage $V_{\rm off}$ and the selection of the (relative) series inductance $L_{\rm s}/L_{\rm s,max}$. Note that designs with $L_{\rm s} < L_{\rm s,min}$ are greyed out. As can be observed, the transformer current stresses (which also define the power transistor current stresses in the ac switching cell, i.e., in M_1, M_2) can be minimized by a *high* offset voltage $V_{\rm off}$ and a low series inductance value $L_{\rm s} = L_{\rm s,min}$, which corresponds to short transformer current direction-reversal intervals (i.a) and (ii.b) in **Fig. 4**. However, the blocking voltage of the power transistors M_1, M_2 is defined by $V_{\rm off}$ and thus, a trade-off exists between transformer / power transistor current stresses and the power transistor voltage stresses / switching losses, which is investigated in detail in **Section III-C**.

In order to assure DAB-type power transfer, the series capacitors $C_{\rm sp}$, $C_{\rm ss}$ (**Fig. 1b**) must show negligible impedance at the switching frequency $f_{\rm sw}$ compared to the transformer series inductance $L_{\rm s}$. Here, a factor of 10 in impedance difference is considered, i.e., $Z_{\rm Ls}(f_{\rm sw}) = 10 \cdot Z_{\rm Csp}(f_{\rm sw})$, resulting in $C_{\rm sp} = 3\,\mu$F for $L_{\rm s} = 16.5\,\mu$H selected in **Section III-C**. The same value is chosen for the primary-side related secondary-side series capacitor $C'_{\rm ss} = \frac{1}{n^2}C_{\rm ss}$, thus resulting in $C_{\rm ss} = 12\,\mu$F for the selected optimum transformer turns ratio of $n = 0.5$ (6).

C. Power Transistors

As discussed, there exists a trade-off between the transformer current stresses and the ac-side power transistor voltage stresses. Further, the transformer current $i_{\rm p}$ directly influences the current stresses of the power transistors $M_1 \ldots M_4$ as

$$i_{\rm M1} = s_1 \cdot (i_{\rm L1} - i_{\rm L2} - i_{\rm p}) \approx s_1 \cdot (2i_{\rm ac} - i_{\rm p}), \tag{13}$$

$$i_{\rm M2} = s_2 \cdot (-i_{\rm L1} + i_{\rm L2} + i_{\rm p}) \approx s_2 \cdot (-2i_{\rm ac} + i_{\rm p}), \tag{14}$$

$$i_{\rm M3} = s_3 \cdot (-i_{\rm s}) = s_3 \cdot (i_{\rm p} \cdot \frac{1}{n}), \tag{15}$$

$$i_{\rm M4} = s_4 \cdot (i_{\rm s}) = s_4 \cdot (-i_{\rm p} \cdot \frac{1}{n}), \tag{16}$$

where $s_{1\ldots4} \in \{0, 1\}$ are the corresponding gate signals.

Thus, there exists a trade-off between the power transistor conduction and switching losses which both depend on the

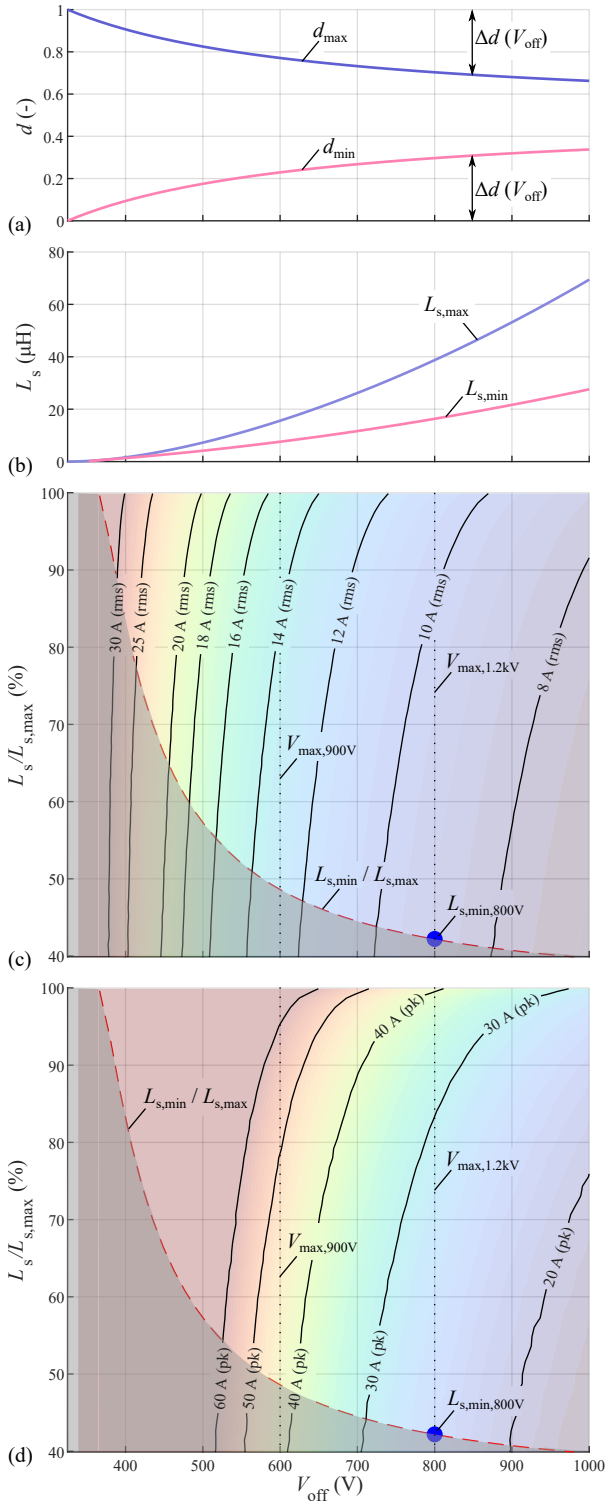

Fig. 5. Design guidelines for the selection of a suitable transformer leakage inductance (the considered circuit specifications are $V_{\mathrm{ac,rms}} = 230\,\mathrm{V}$ (line-to-neutral), $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$, $V_{\mathrm{dc}} = 400\,\mathrm{V}$, $P_{\mathrm{ac}} = 2.5\,\mathrm{kW}$ and $f_{\mathrm{sw}} = 72\,\mathrm{kHz}$): Impact of the offset voltage V_{off} on **(a)** minimum d_{min} and maximum d_{max} values of the duty cycle d within one grid period, **(b)** maximum and minimum value for the transformer series inductance L_{s}. **(c)** and **(d)** further investigate the rms and maximum peak transformer currents $I_{\mathrm{p,rms}}$ and $\hat{I}_{\mathrm{p}}$, respectively, in dependence of the offset voltage V_{off} and the relative series inductance $\frac{L_{\mathrm{s}}}{L_{\mathrm{s,max}}}$ (the maximum tolerable offset voltages V_{off} for 900 V as well as 1.2 kV SiC MOSFETs considering a 33% blocking voltage margin are highlighted).

selected transformer series inductance L_{s} and the ac switching cell offset voltage V_{off}. To determine the optimum offset voltage V_{off} resulting in minimum total power transistor losses (i.e., including the conduction and switching losses of the ac-side M_1, M_2 and dc-side M_3, M_4 power transistors), a power transistor chip area optimization is done for various offset voltages V_{off} and leakage inductance values $L_{\mathrm{s}} \in [L_{\mathrm{s,min}}, L_{\mathrm{s,max}}]$.

The considered SiC power MOSFETs are listed in **Tab. III** where also the corresponding sources for accurate calorimetric switching loss measurement data are given. Depending on the offset voltage, either 900 V (C3M0010090K; $V_{\mathrm{off}} \leq 600\,\mathrm{V}$) or 1.2 kV (C3M0016120K; $V_{\mathrm{off}} \leq 800\,\mathrm{V}$) are considered for the realization of the ac-side switches M_1, M_2 to assure a 33% blocking voltage margin. Note that, similar to a conventional half-bridge configuration, the voltage across M_1 and M_2 is well defined and a compact power commutation loop is formed by the capacitors C_1 and C_2 (see **Fig. 1b**). The number of parallel-connected power transistors devices for the realization of M_1 and M_2 is varied with $N_{\mathrm{par}} \in [0.5, 4]$ to explore the trade-off between switching and conduction losses. Values $N_{\mathrm{par}} < 1$ are also considered to account for the availability of power transistors with higher on-state resistance values based on the same technology.

The dc-side power transistors M_3, M_4 are blocking the dc output voltage $V_{\mathrm{dc}} = 400\,\mathrm{V}$ (independently of the offset voltage V_{off}), and 650 V SiC MOSFET technology (IMZA65R027M1H) can be considered. As the dc-side power transistors are fully soft switched, the switching losses are extremely low and it is advantageous to maximize the chip area within economic limits. Thus, the lowest on-state resistance available (for the considered series) in a single TO-247-4 package (IMZA65R015M2H) of $14.5\,\mathrm{m\Omega}$ is selected for M_3, M_4 ($N_{\mathrm{par}} = 1.86$ with respect to IMZA65R027M1H).

Fig. 6a shows the resulting minimum total conduction and switching losses of the power transistors $M_1 \ldots M_4$ (i.e., resulting with optimum N_{par} for the ac-side power transistors M_1 and M_2) in dependence of the offset voltage V_{off} and leakage inductance values L_{s}, where a constant power transistor junction temperature of 120 °C is assumed. Note that only values $V_{\mathrm{off}} \geq 400\,\mathrm{V}$ are displayed to avoid excessively high current stresses and losses. As can be observed, the power transistor losses are minimum when selecting $L_{\mathrm{s}} = L_{\mathrm{s,min}}$ across the entire range of V_{off} due to the reduced transformer current stresses (see **Figs. 5c,d**).

Thus, **Fig. 6b** considers $L_{\mathrm{s}} = L_{\mathrm{s,min}}$ (i.e., minimal losses) and, for each offset voltage level V_{off}, further details the optimal on-state resistance $R_{\mathrm{ds,on}} = R_{\mathrm{nom}}/N_{\mathrm{par}}$ of the ac-side power transistors, and the corresponding calculated conduction P_{c} and switching losses P_{sw} of the ac-side (M_1, M_2) and dc-side (M_3, M_4) power transistors. As can be observed, the switching and conduction losses of the dc-side power transistors M_3, M_4 continuously drop with increasing offset voltage V_{off} due to the lower current stresses (see **Figs.5c,d**). Due to the hard-switching operation, the losses of the ac-side transistors M_1, M_2 are substantially higher than the dc-side losses. The ac switching cell losses also initially decrease rapidly due to the decrease in current stresses (also allowing to utilize smaller chip areas

and/or increasing values of $R_{\mathrm{ds,on,ac}}$ with associated lower hard-switching losses) as the offset voltage V_{off} increases. A step in losses by approximately $-5\,\mathrm{W}$ results at $V_{\mathrm{off}} = 600\,\mathrm{V}$ which is the boundary of the $900\,\mathrm{V}$ and the $1.2\,\mathrm{kV}$ SiC MOSFET technology. Note that surprisingly the $1.2\,\mathrm{kV}$ MOSFET shows superior performance in this application which might be related to the fact that the considered $900\,\mathrm{V}$ MOSFETs evaluated in [17] are engineering samples which may not yet meet the theoretical switching loss performance target. For voltages $V_{\mathrm{off}} > 600\,\mathrm{V}$ the losses marginally increase again due to increasing switching losses with higher switched voltage (V_{off}). Finally, an offset voltage of $V_{\mathrm{off}} = 800\,\mathrm{V}$ is selected as, first, a good utilization of the $1.2\,\mathrm{kV}$ SiC MOSFET technology results and the optimal on-state resistance $R_{\mathrm{ds,on,ac}} = 16\,\mathrm{m\Omega}$ can be realized without parallel connecting several discrete devices ($N_{\mathrm{par}} = 1$), and second, an optimum transformer turns ratio 2:1 ($n = 0.5$ (6)) results.

The corresponding ideal transformer leakage inductance $L_{\mathrm{s}} = L_{\mathrm{s,min}} = 16.5\,\mu\mathrm{H}$ is highlighted with a blue marker in **Figs. 5c,d**, resulting in $\hat{I}_{\mathrm{p}} = 24.1\,\mathrm{A}$ and $I_{\mathrm{p,rms}} = 8.9\,\mathrm{A}$. The total calculated power transistor losses of $M_1 \dots M_4$ at nominal load are about $46\,\mathrm{W}$ and correspond to an expected semiconductor efficiency of 98.2%.

D. DC-Link

Assuming a constant output power $P_{\mathrm{dc}} = P_{\mathrm{ac}}$, the twice-grid-frequency energy variation buffered by the dc-link capacitor ΔE_{dc} can be expressed by

$$\Delta E_{\mathrm{dc}} = \frac{\frac{1}{2}\hat{V}_{\mathrm{ac}}\hat{I}_{\mathrm{ac}}}{2\pi f_{\mathrm{ac}}}. \tag{17}$$

To maintain a maximum peak-to-peak dc-link voltage variation $\Delta V_{\mathrm{dc}} = 10\,\mathrm{V}$ (i.e., $V_{\mathrm{dc}} \in [395\,\mathrm{V}, 405\,\mathrm{V}]$), the required dc-link capacitance can be approximated with

$$C_{\mathrm{dc}} \approx \frac{\Delta E_{\mathrm{dc}}}{V_{\mathrm{dc}} \Delta V_{\mathrm{dc}}} = 2\,\mathrm{mF}. \tag{18}$$

E. Performance Analysis

The calculated power semiconductor efficiency is 98.2% (see above). The total losses of the inductors and the transformer, are highly dependent on the specific realization of the components and a trade-off exists between compactness and efficiency of these passives [19], [20]. Aiming at a rough performance estimation, the losses relative to the processed power are estimated as 1% for the transformer and 0.5% for each inductor L_1 and L_2. The losses of the filter capacitors C_1, C_2 and series capacitors C_{sp}, C_{ss} are assessed assuming a loss tangent $\tan(\delta) = 0.1\%$. It is conservatively assumed that the entire HF rms capacitor current of $12.9\,\mathrm{A}$ for the filter capacitors C_1, C_2 occurs at the switching frequency f_{sw}, resulting in losses below $100\,\mathrm{mW}$ in each capacitor. The losses of the series capacitors C_{sp} ($8.8\,\mathrm{A}$) and C_{ss} ($17.9\,\mathrm{A}$) are assessed in the same way and also result below $100\,\mathrm{mW}$. For the dc output capacitor C_{dc}, the LF losses at $2f_{\mathrm{ac}}$ are calculated assuming an electrolytic capacitor with $\tan(\delta) = 0.1$ and result in $1.6\,\mathrm{W}$. Considering further auxiliary losses (controller, measurement circuitry, gate drives, fans) of $5\,\mathrm{W}$, the estimated losses at the nominal load of $2.5\,\mathrm{kW}$ total to $103\,\mathrm{W}$ corresponding to an overall efficiency of about 95.9%.

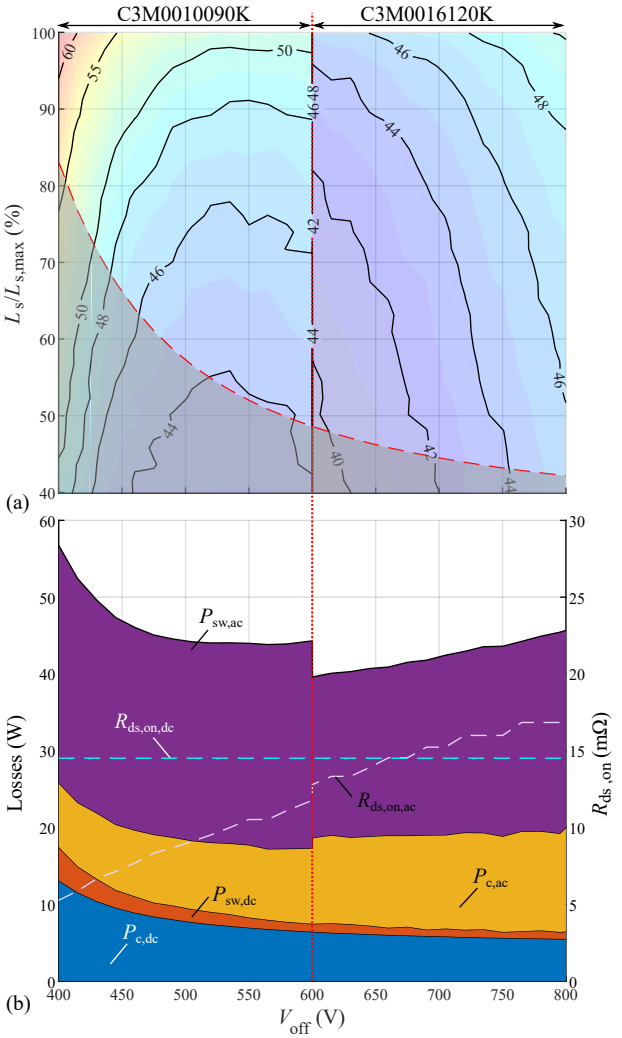

Fig. 6. Chip area optimization for the realization of the ac-side M_1, M_2 and dc-side M_3, M_4 power transistors. The considered SiC MOSFETs and references to the loss models are listed in **Tab. III**. A constant junction temperature of $120\,^{\circ}\mathrm{C}$ is assumed for the calculation. **(a)** Minimum total power transistor losses (switching and conduction) of $M_1 \dots M_4$ depending on the offset voltage V_{off} and the relative leakage inductance $L_{\mathrm{s}}/L_{\mathrm{s,max}}$. **(b)** Detailed switching P_{sw} and conduction P_{c} loss distribution, and optimum on-state resistances $R_{\mathrm{ds,on}}$ for the ac- and dc-side transistors depending on V_{off} for $L_{\mathrm{s}} = L_{\mathrm{s,min}}$. Note that $R_{\mathrm{ds,on,dc}} = const.$

This is similar to the 95.6% that have been reported for a single-stage isolated ac-dc Ćuk converter [21], which can also be realized with only four switches. Comparing with state-of-the-art systems, e.g. the combination of [22] with [23] or the single-stage system [6], which achieve an overall efficiency of about 98%, the trade-off between high efficiency (**Fig. 1a**) and lower active-component-count (**Fig. 1b**) becomes apparent, even if a detailed comparison should consider systems with similar power density.

IV. Control

To realize a sinusoidal grid current i_{ac} and dc output voltage control, three control loops are required as highlighted in **Fig. 7:** The dc output voltage PI controller defines an (average) power reference depending on the instantaneous dc output voltage error $V_{\mathrm{dc}} - V_{\mathrm{dc}}^{*}$, which is translated into a sinusoidal grid current reference i_{ac}^{*} in phase with the grid voltage v_{ac} via a reference

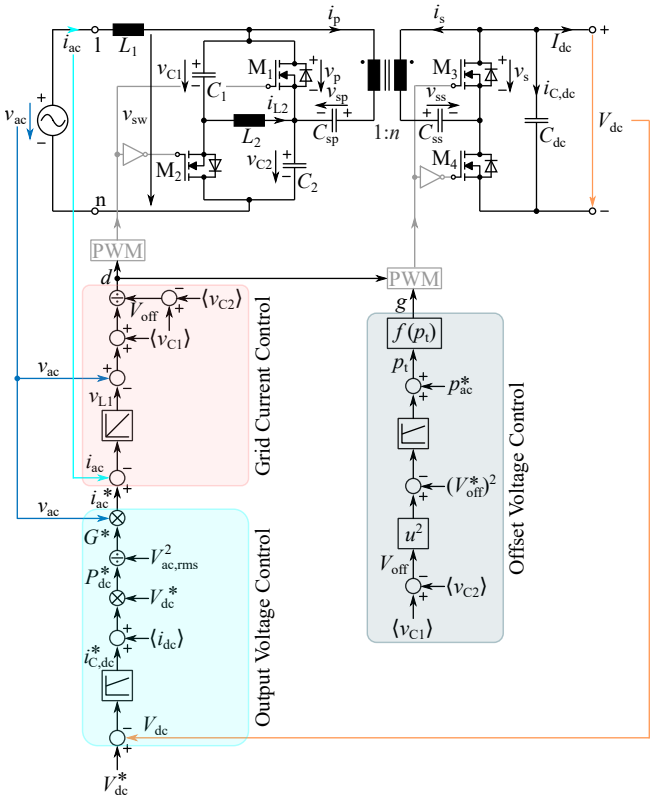

Fig. 7. Control scheme for the novel single-stage PFC rectifier with high-frequency isolation from **Fig. 1b**. Highlighted are the three controllers for the output voltage (blue, with PI gains $k_{\mathrm{p,dc}} = 0.109\,\mathrm{A/V}$, $k_{\mathrm{i,dc}} = 3.95\,\mathrm{A/Vs}$), the grid current (red, with gain $k_{\mathrm{p,grid}} = 20.4\,\mathrm{V/A}$), and the offset voltage (grey, with PI gains $k_{\mathrm{p,off}} = 0.0117\,\mathrm{W/V^2}$, $k_{\mathrm{i,off}} = 30.5\,\mathrm{W/V^2 s}$).

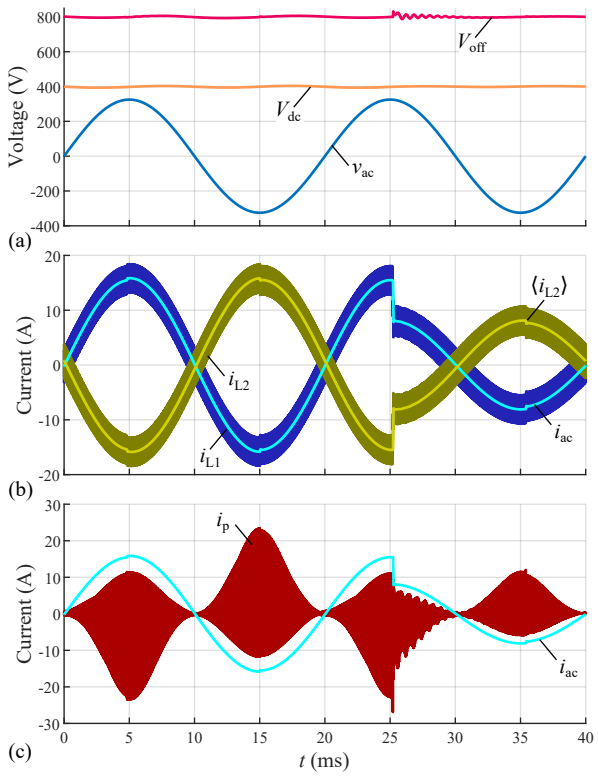

Fig. 8. Simulated waveforms during two mains periods with $V_{\mathrm{ac,rms}} = 230\,\mathrm{V}$ (line-to-neutral), $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$, $V_{\mathrm{dc}} = 400\,\mathrm{V}$ and the converter parameters listed in **Tab. II**. The dc-side load is modeled by a controlled current source which adjusts the dc load current I_{dc} from 6.25 A to 3.125 A (corresponding to a power change from 2.5 kW to 1.25 kW) at $t = 25\,\mathrm{ms}$. **(a)** Input v_{ac}, output V_{dc} and offset voltage V_{off}, **(b)** inductor i_{L1}, i_{L2} and grid current i_{ac}, and **(c)** primary-side transformer current i_{p} and grid current i_{ac}.

conductance G^*. The grid current i_{ac} is tracked by means of a simple proportional controller which marginally adjusts the duty cycle d (defining the relative on-time of M_1) from its feed-forward value defined in (3). A third control loop adjusts the PWM carrier phase-shift g to assure that the offset voltage $V_{\mathrm{off}} = v_{\mathrm{C1}} - v_{\mathrm{C2}}$ is equal to its reference value $V^*_{\mathrm{off}} = 800\,\mathrm{V}$, using the grid input power reference $p_{\mathrm{ac}} = i^*_{\mathrm{ac}} v_{\mathrm{ac}}$ as a feed-forward term. Essentially, regulating the offset voltage to a constant value ensures that the characteristic single-phase power flow pulsating with twice the mains frequency is transferred to the dc output, where the fluctuation is buffered in C_{dc} as discussed above. Note that a single controller is sufficient to control the offset voltage as the auxiliary inductor L_2 assures an equal offset voltage sharing of $V_{\mathrm{off}}/2$ of capacitors C_1 and C_2.

V. Simulation Results

To verify the proposed converter concept, a detailed circuit simulation, including closed-loop control and using the parameters from **Tab. II** has been implemented in PLECS. **Fig. 8** depicts the resulting main converter waveforms for operation in the 50 Hz, 230 V (rms, line-to-neutral) European single-phase ac grid where a sinusoidal grid current and unity power factor can be observed. A load step from $P_{\mathrm{ac}} = 2.5\,\mathrm{kW}$ to $P_{\mathrm{ac}} = 1.25\,\mathrm{kW}$ is applied at around $t = 25\,\mathrm{ms}$ and the controller rapidly tracks the new power reference while maintaining stable offset V_{off} and dc output V_{dc} voltage.

Simulation results of the system startup are presented in **Fig. 9**. Before connecting the PFC rectifier to the grid, all capacitors are discharged and no power is available for the control circuits, and thus we propose a safe and fast four-step converter startup sequence. At time $t_0 = 0\,\mathrm{ms}$ (where $v_{\mathrm{ac}} = \hat{V}_{\mathrm{ac}}$), the rectifier is connected to the grid voltage via a precharge resistor $R_{\mathrm{pre}} = 20\,\Omega$, which limits the inrush current to $< 20\,\mathrm{A}$, and an offset voltage $V_{\mathrm{off}} = \hat{V}_{\mathrm{ac}}$ naturally establishes. Note that at this point no load is connected at the dc output terminals. At $t_1 = 20\,\mathrm{ms}$ the precharge resistor is bypassed, and the grid current controller and the dc output voltage controller are activated. Note that here only the PWM signals of the ac switching cell M_1 and M_2 are enabled, while M_3 and M_4 remain off and their body diodes act as a passive rectifier. The output voltage reference V^*_{dc} is ramped up from 0 V to the nominal voltage of 400 V during 200 ms. This leads to an increase in the offset voltage V_{off}, which is not yet actively controlled and thus shows a $2f_{\mathrm{ac}}$ voltage fluctuation due to the single-phase grid power pulsation. At $t_2 = 160\,\mathrm{ms}$, V_{off} exceeds the threshold value of 700 V and PWM signals of the dc-side power transistors M_3 and M_4, and the offset voltage regulator are activated such that a DAB-type HF power transfer results. The offset voltage is rapidly regulated to the set point of 800 V and the dc voltage ramp is continued in parallel. Finally, at $t_3 = 225\,\mathrm{ms}$ the nominal dc output voltage

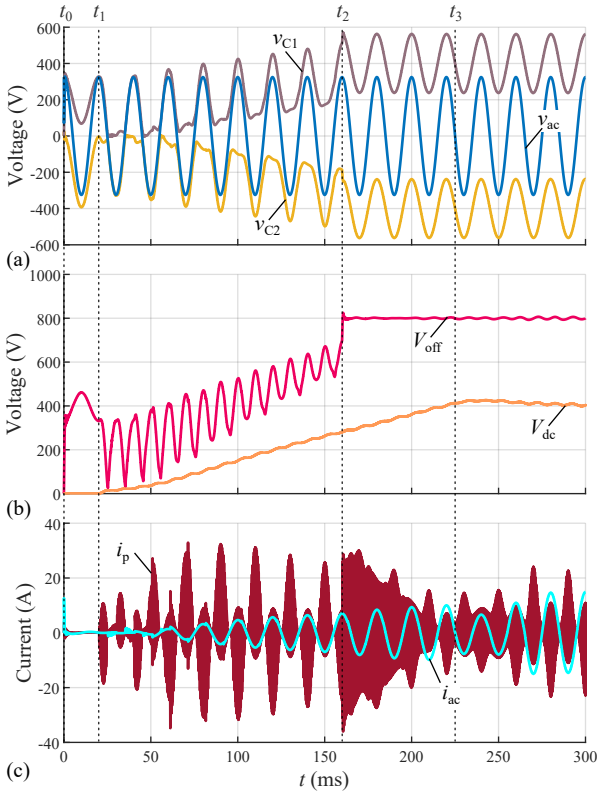

Fig. 9. Startup sequence; details see text. **(a)** Input voltage v_{ac}, capacitor voltages v_{C1} and v_{C2}, **(b)** offset voltage V_{off} and output voltage V_{dc}, and **(c)** transformer current i_p and grid current i_{ac}.

of 400 V is reached. Then, the load current/power is ramped up to the nominal power of 2.5 kW within two grid periods.

VI. Conclusion

Single-phase PFC rectifiers supplying a dc bus voltage common for several variable speed motor drive inverters should not only provide galvanic isolation but also allow for bidirectional power flow. State-of-the-art topologies usually suffer from either high active component count and/or a two-stage power conversion. To overcome these shortcomings, this paper presents a single-stage single-phase PFC rectifier with integrated HF galvanic isolation. The topology has been proposed in [13], however without providing a detailed analysis of the converter design and realization aspects. Thus, in this paper, the operating principle is discussed in depth. Detailed design guidelines for the dimensioning of the main power components for a 2.5 kW prototype system are provided. Based on a power transistor chip-area optimization, a nominal semiconductor efficiency of 98% is expected; and the estimated total system efficiency is close to 96%, i.e., in line with other low-active-component-count topologies [21], and, compared to other state-of-the-art systems, this efficiency highlights the trade-off between performance and active component count. Last, a closed-loop control and system start-up strategy is proposed and verified by means of detailed circuit simulations, thus paving the way for a prototype realization to experimentally verify the predicted performance metrics.

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